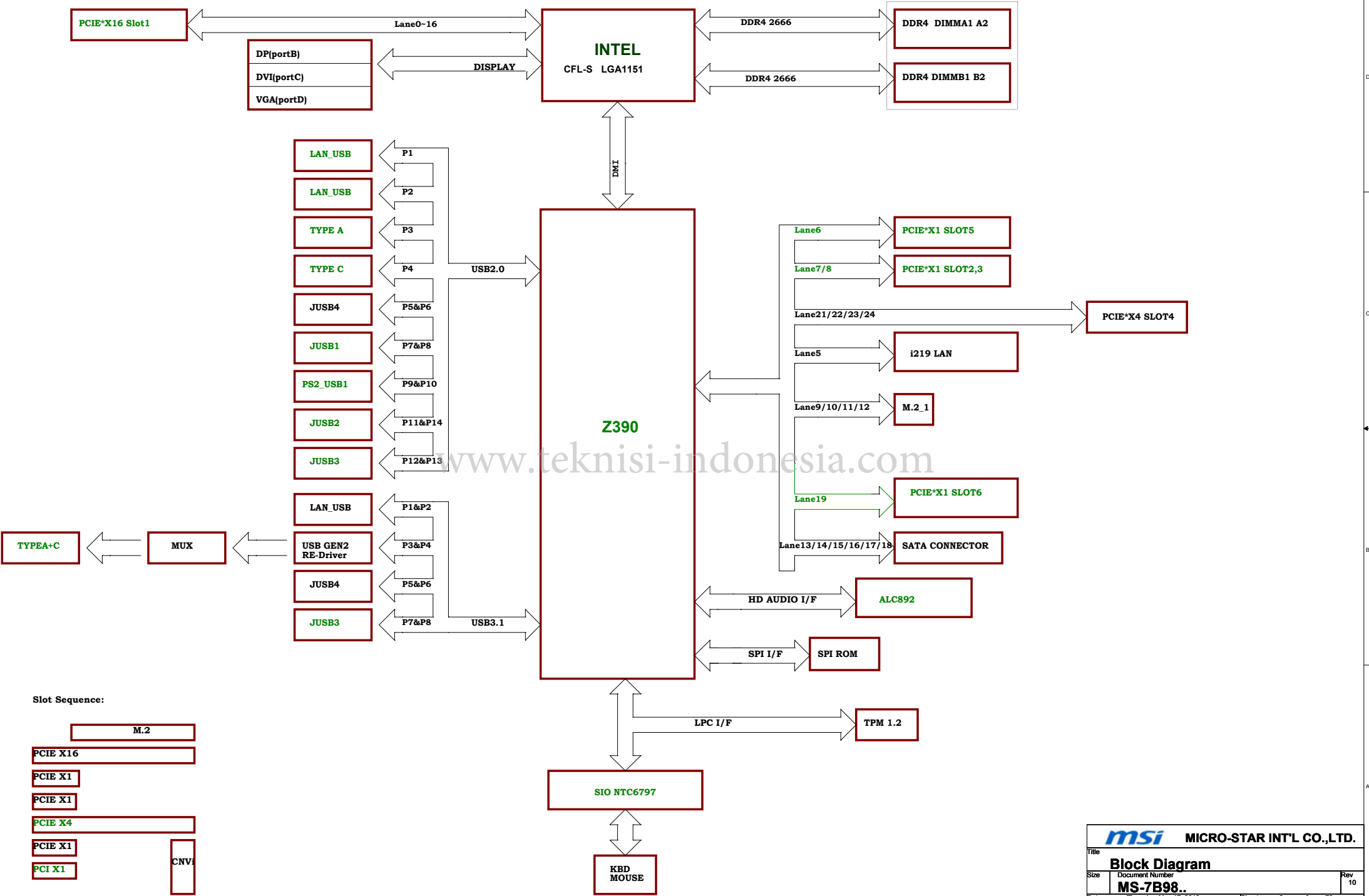
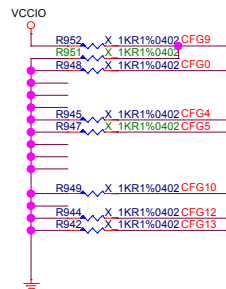
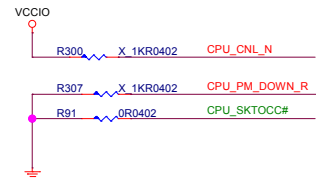
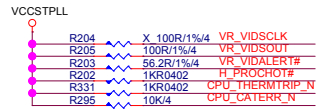




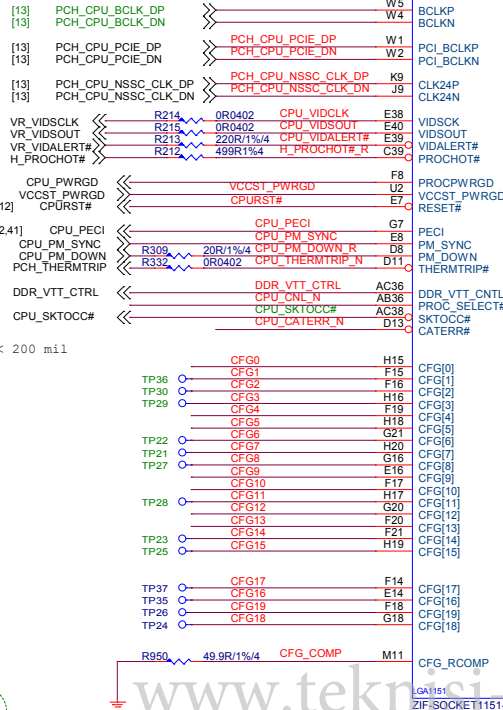
MS-7B98 Block Diagram



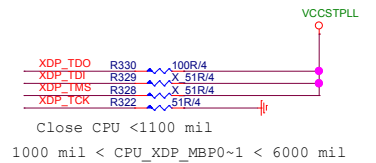
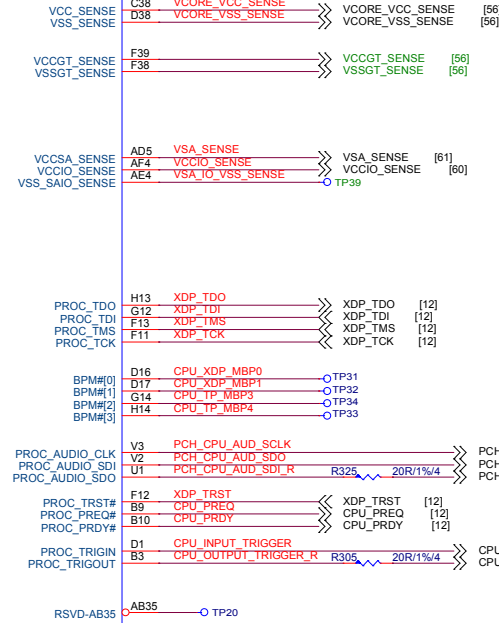


2017/7/13  
Remove JP1 because JP1 combine to J1  
Please see the D78 on page 54

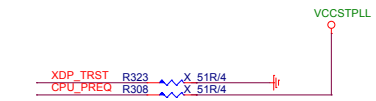
CPU\_PM\_DOWN\_R < 200 mil



## CPU1E CFL-S



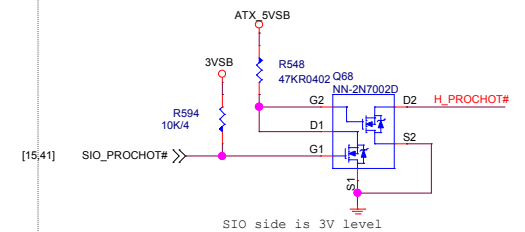
Close CPU <1100 mil  
1000 mil < CPU\_XDP\_MBP0~1 < 6000 mil



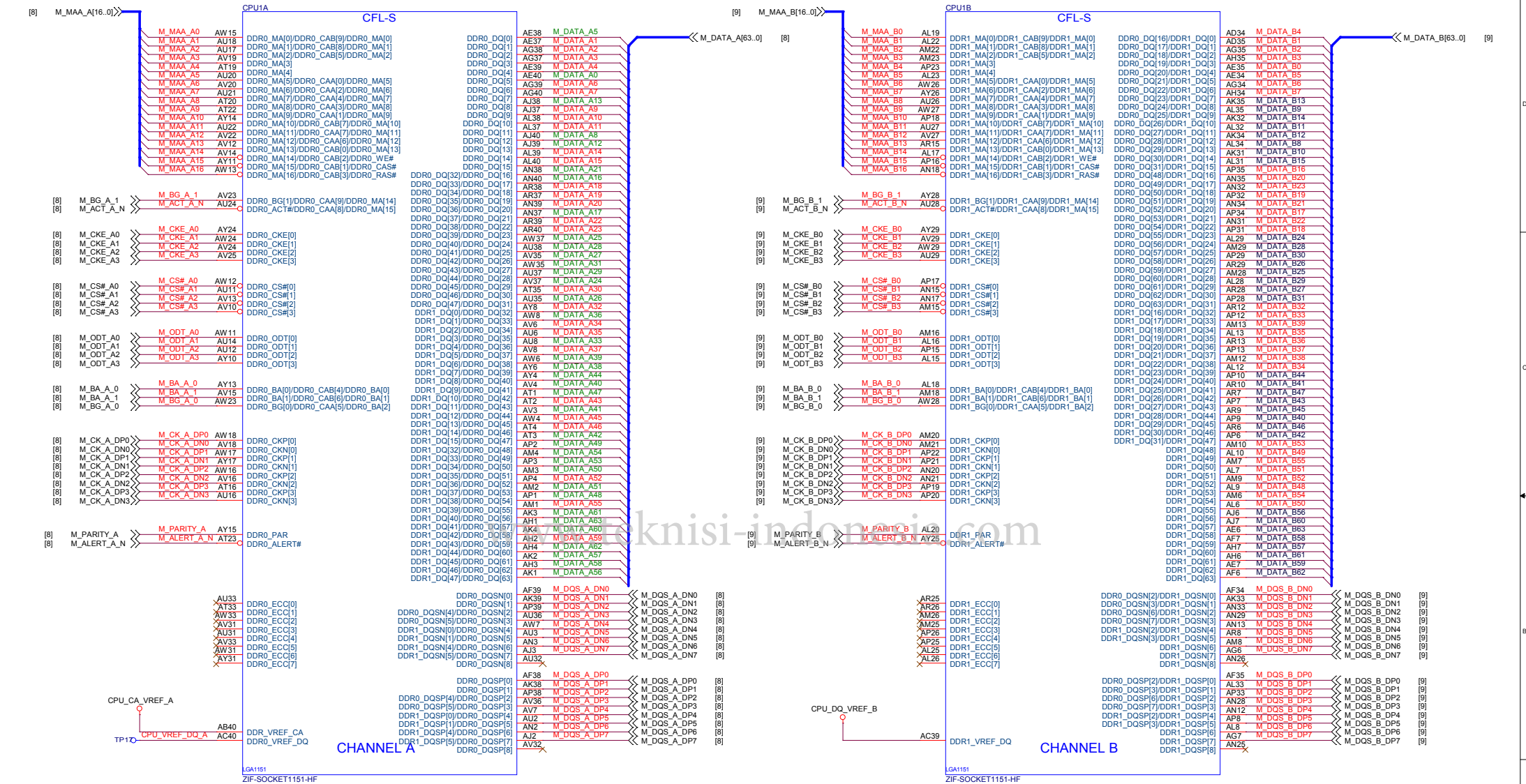
## CFG Strap

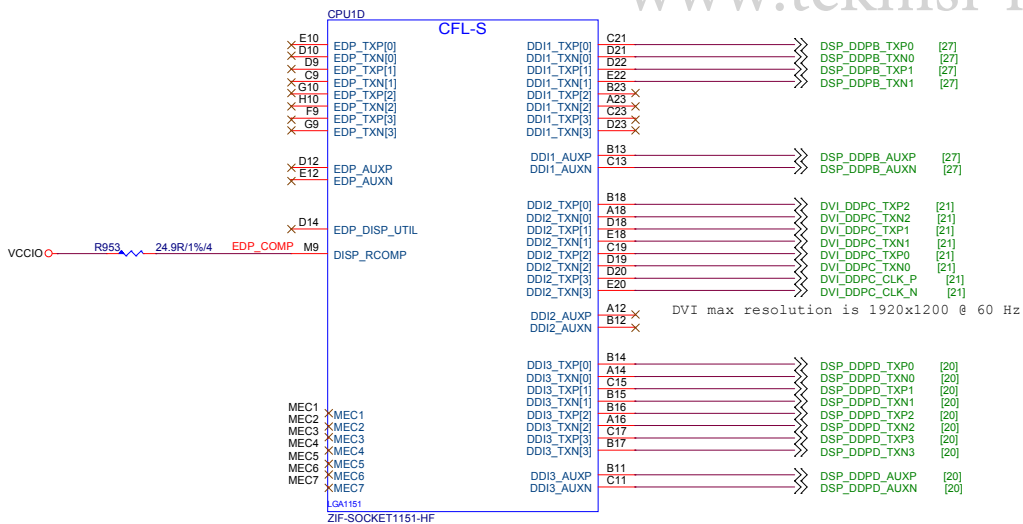
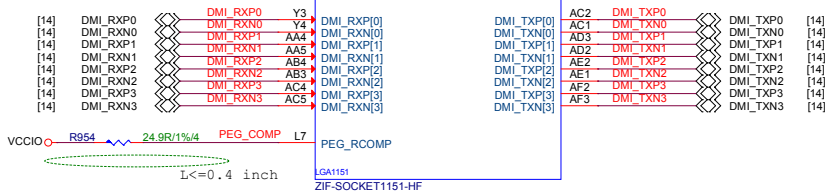
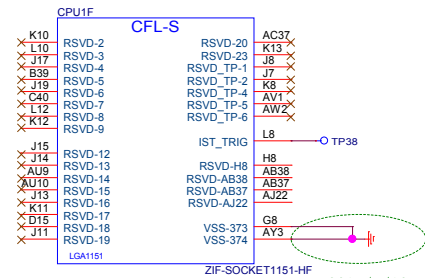
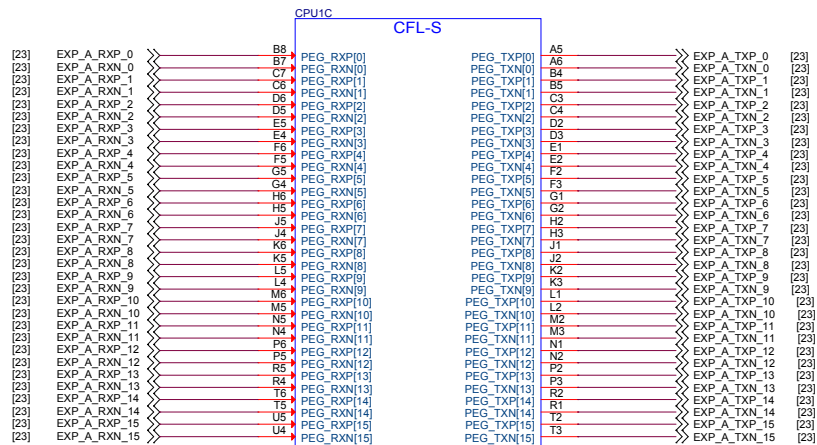
CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEGCFGSEL[0]
6	DISABLE	ENABLE	PEGCFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

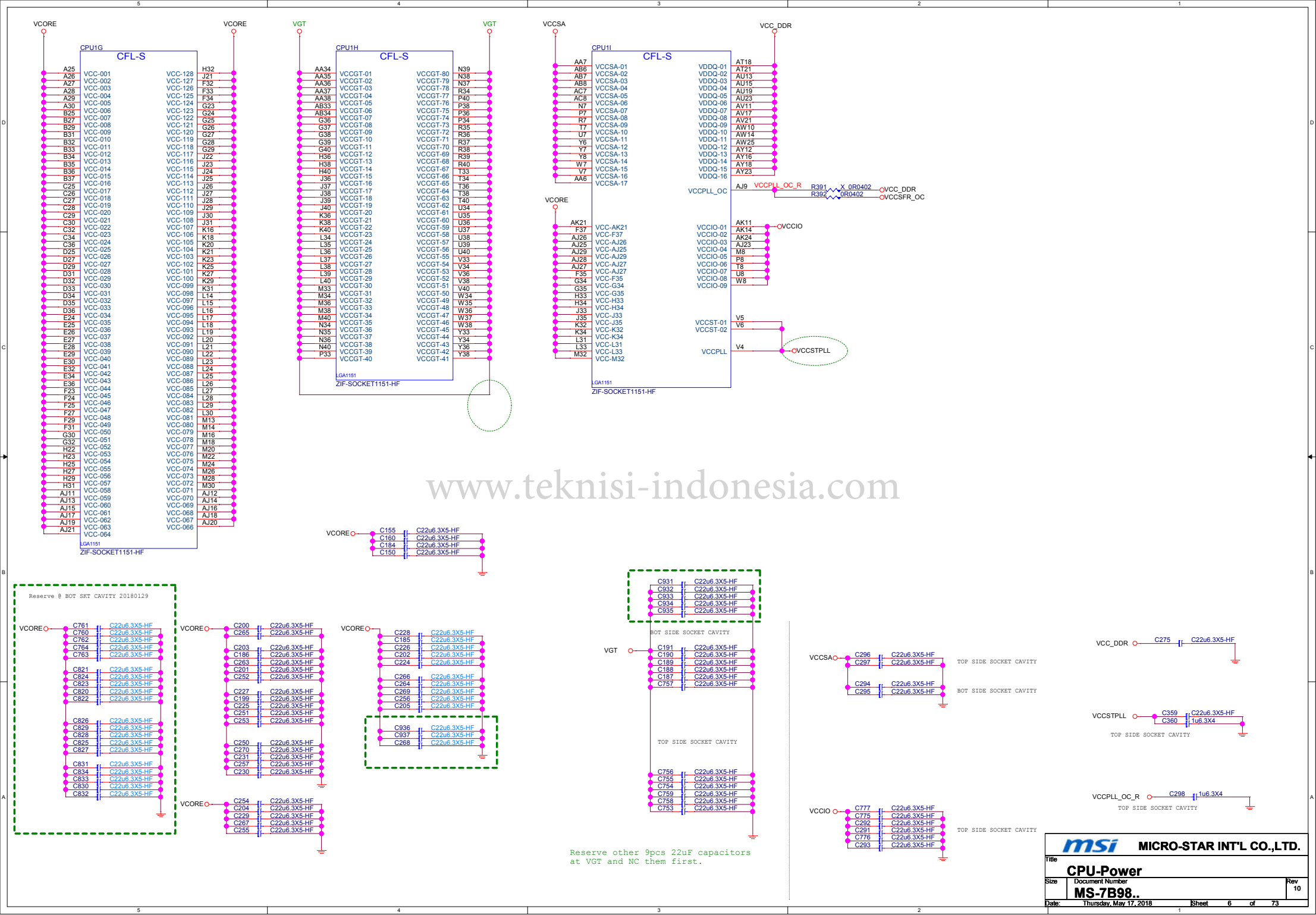


SIO side is 3V level

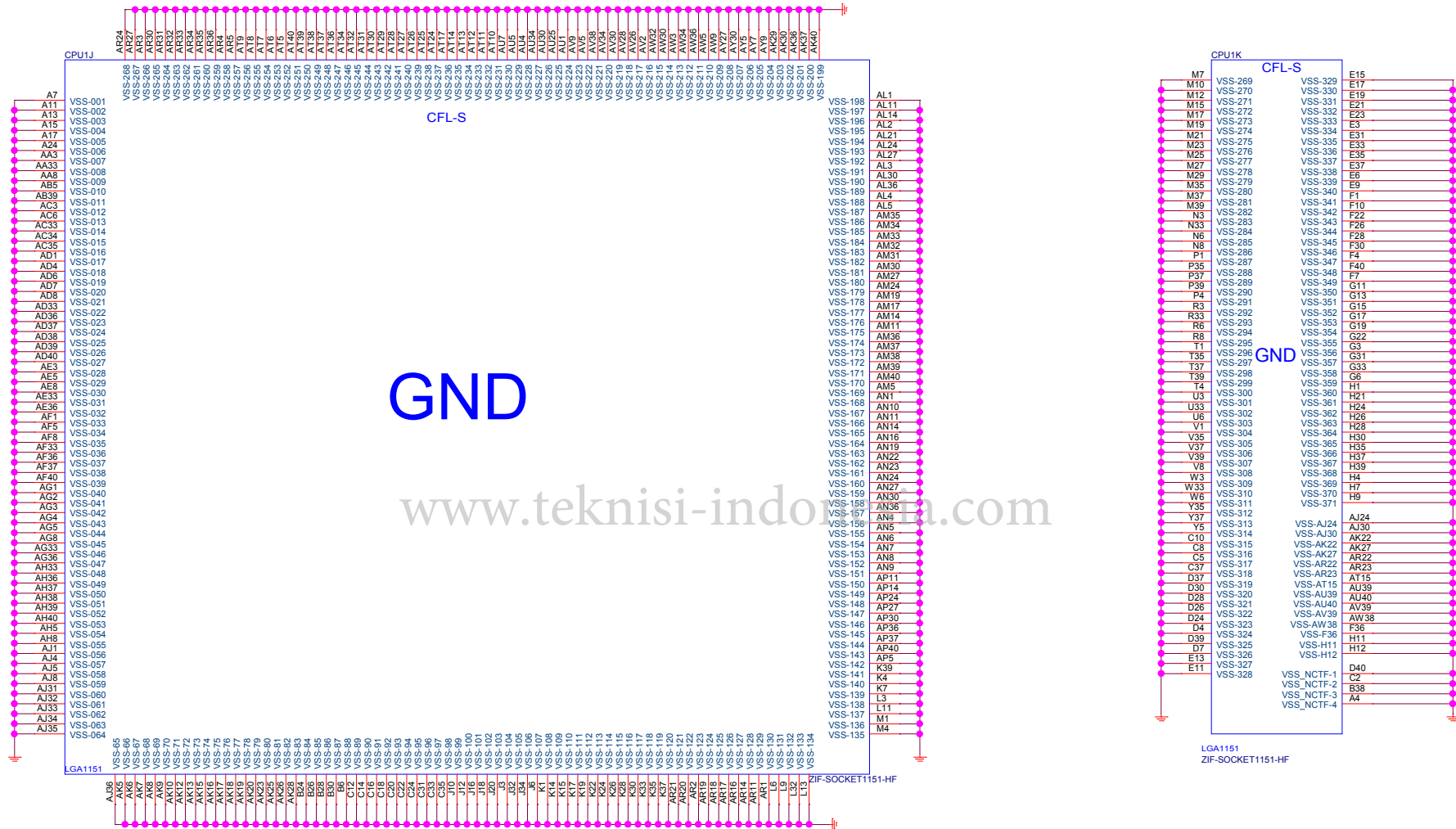


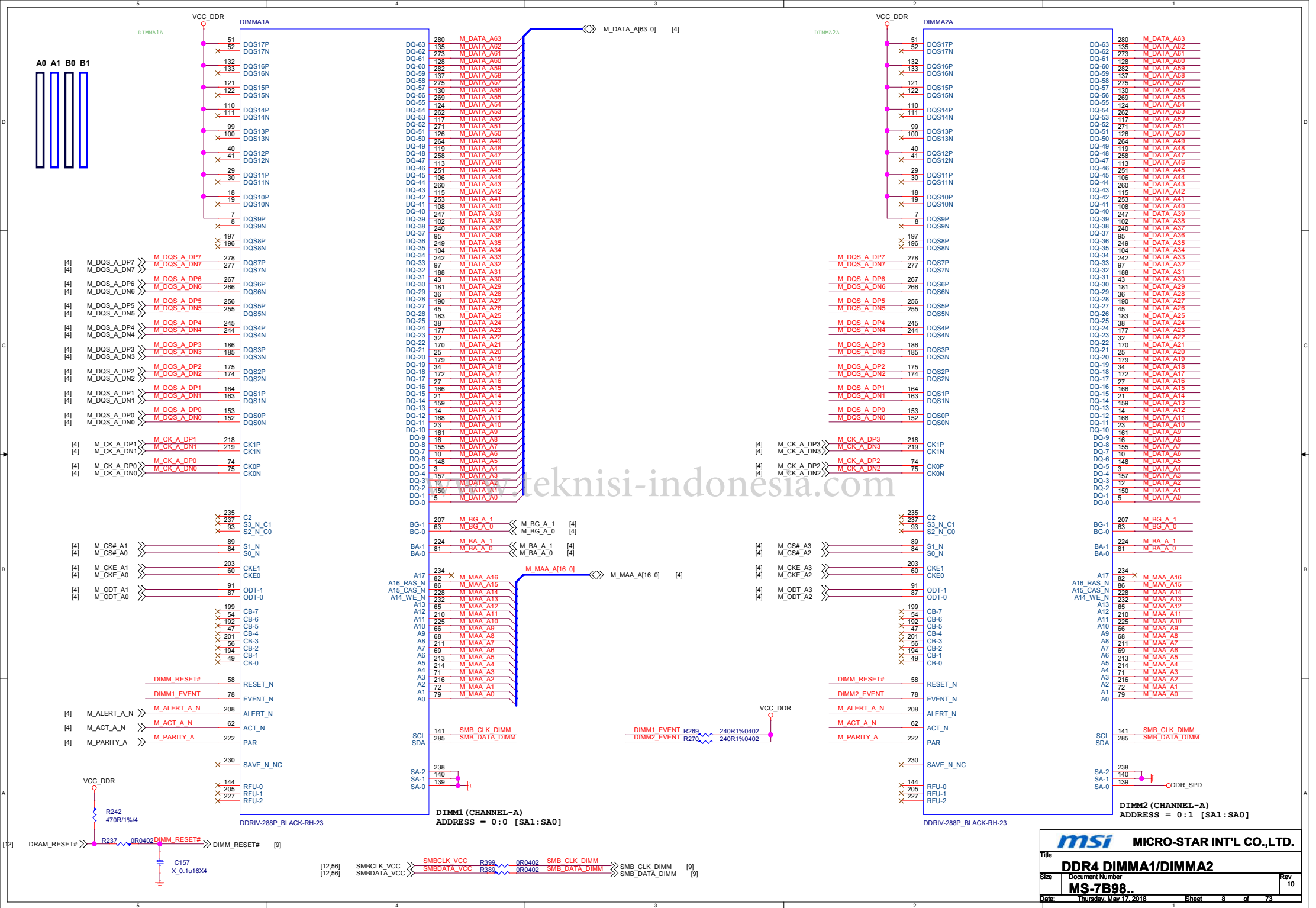


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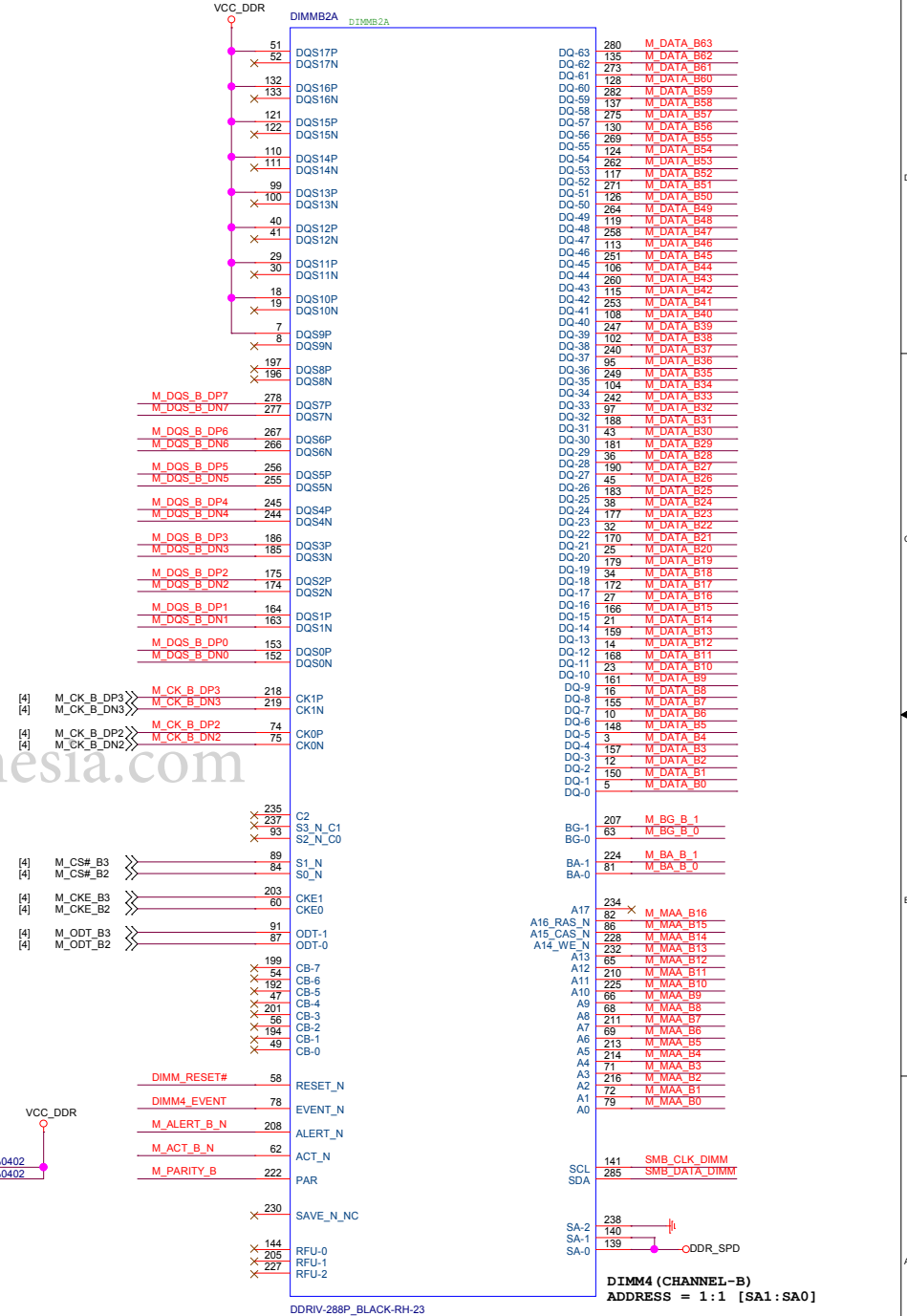
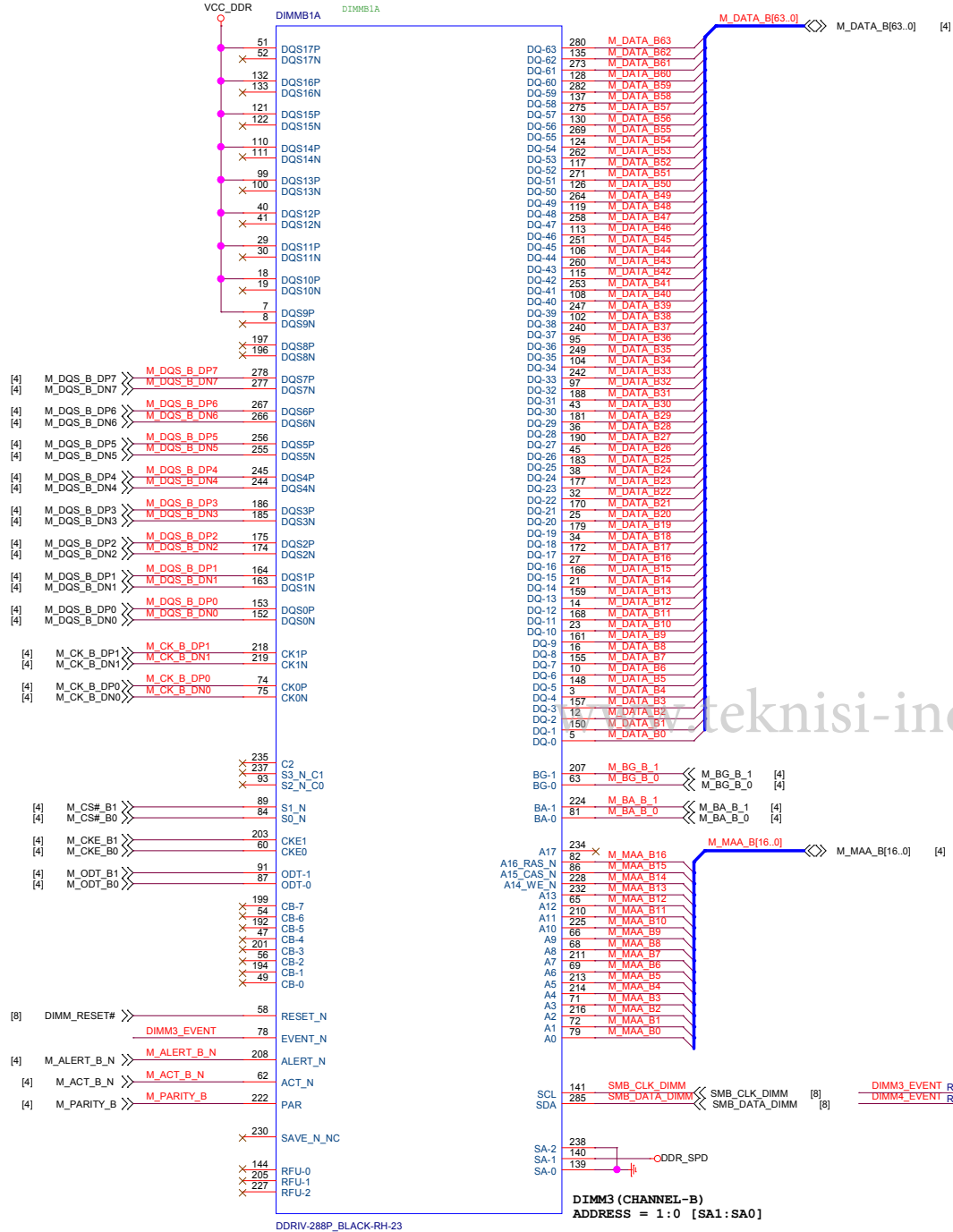


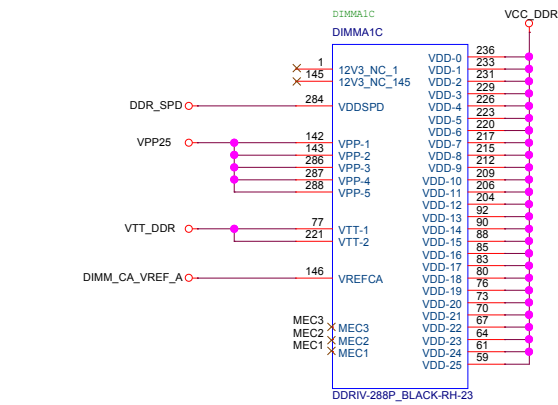




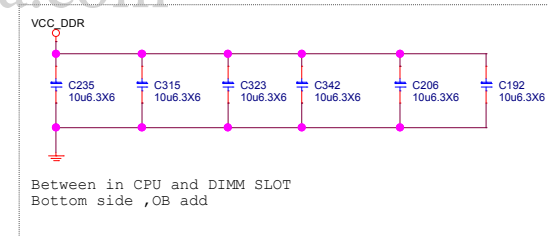
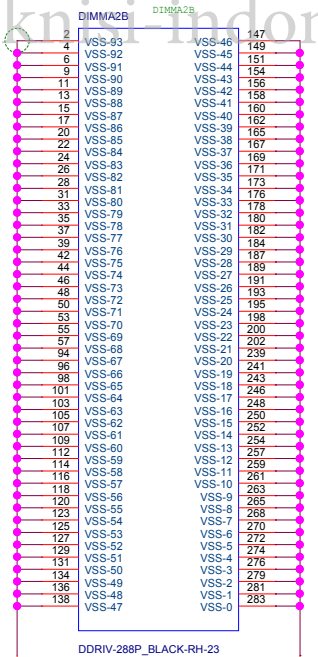
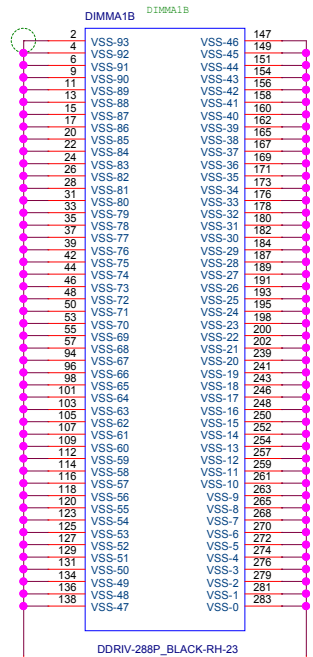
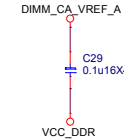
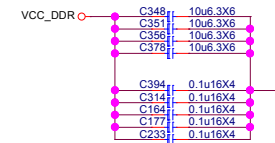
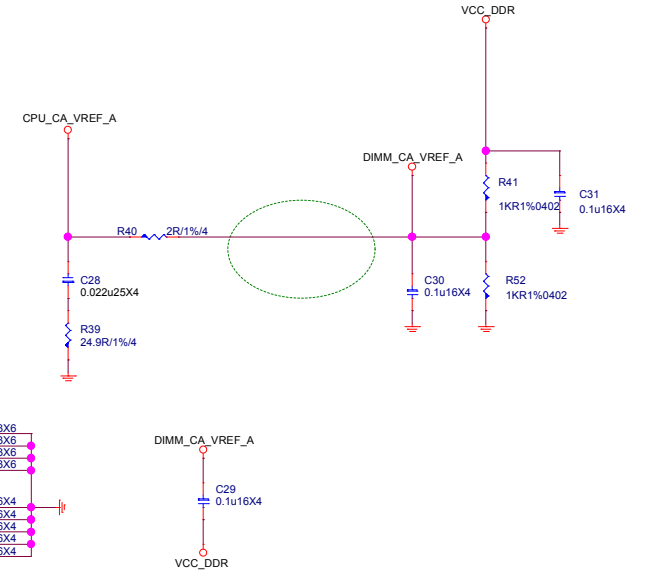
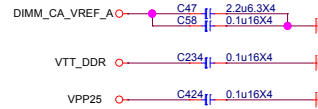
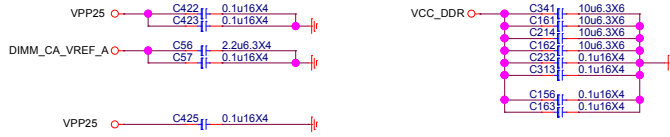
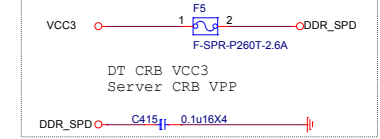
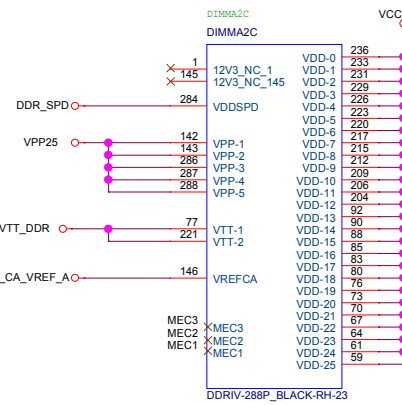
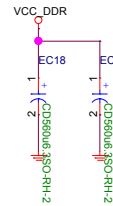




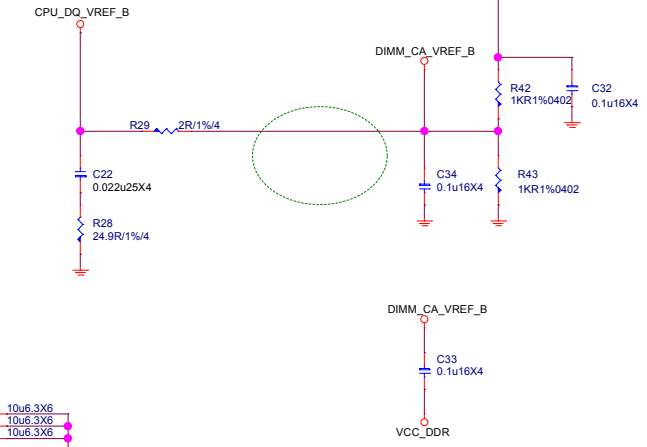
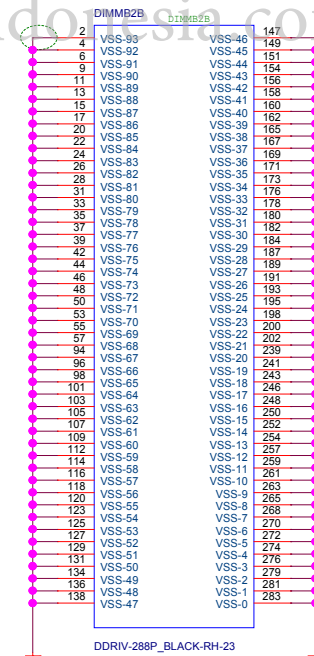
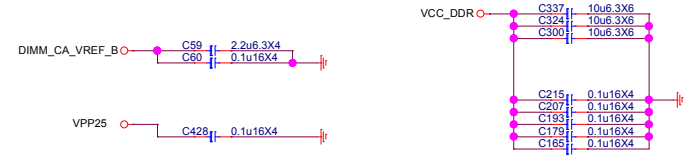
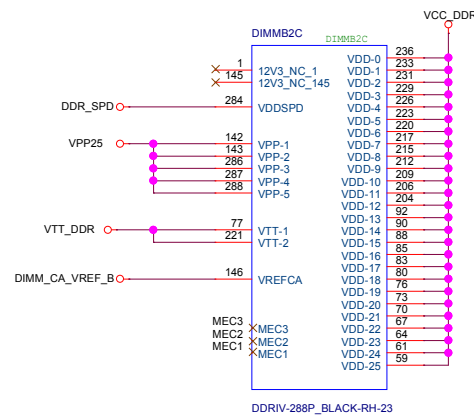
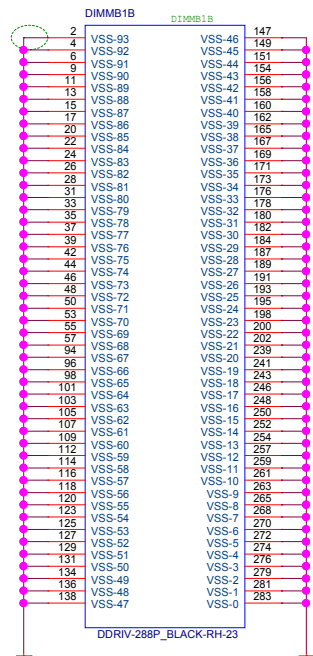
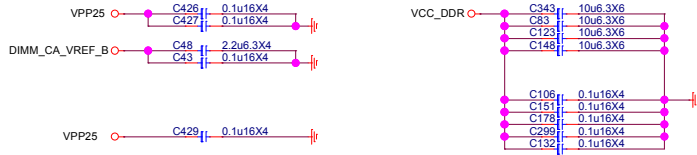
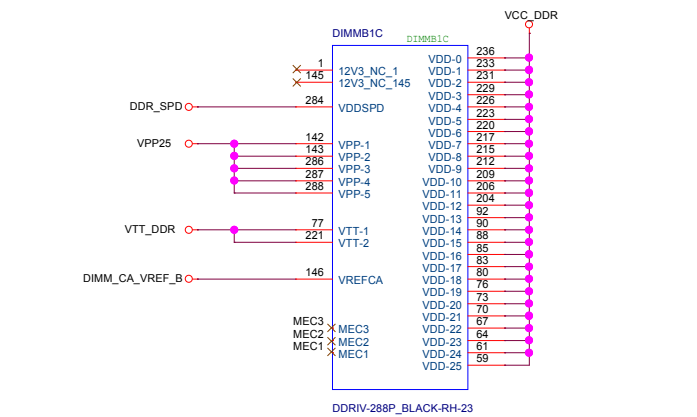




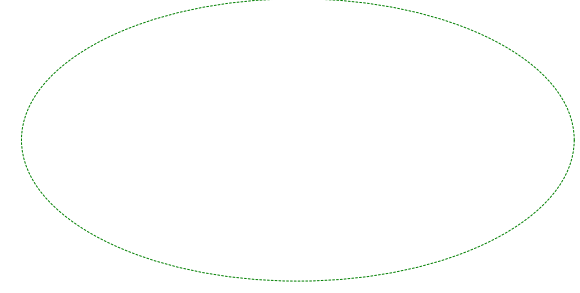
# DIMM SLOT PN BY SPEC

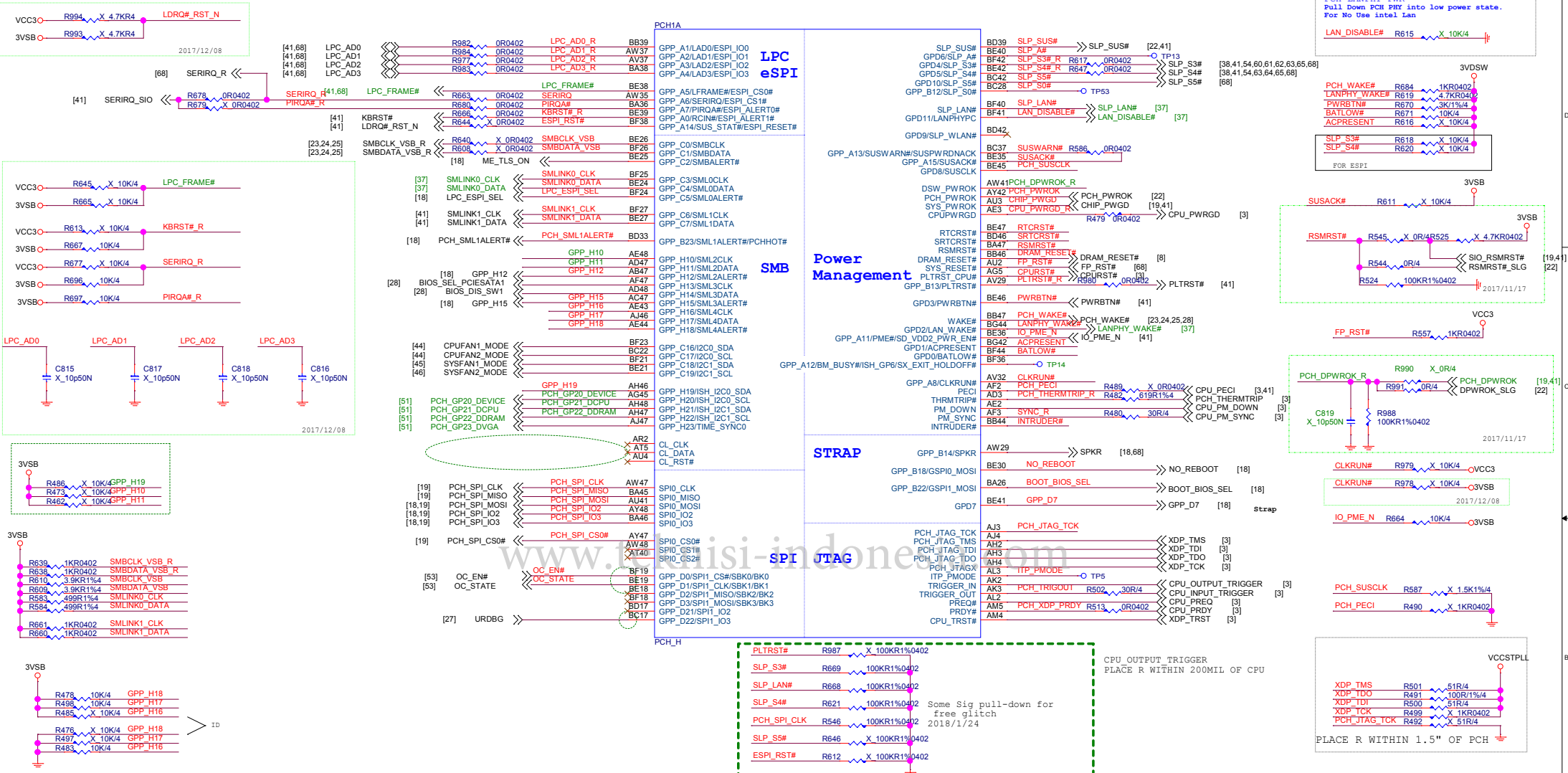


Between in CPU and DIMM SLOT  
Bottom side ,OB add

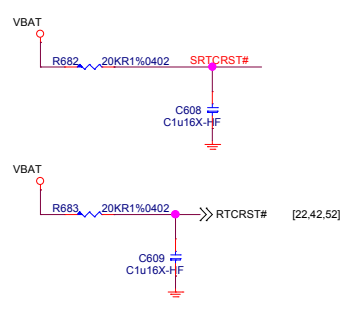


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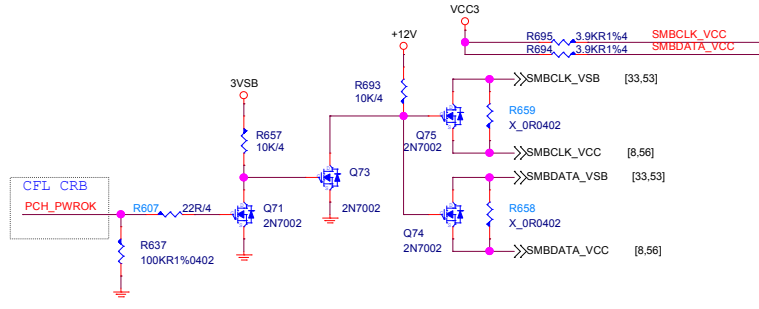
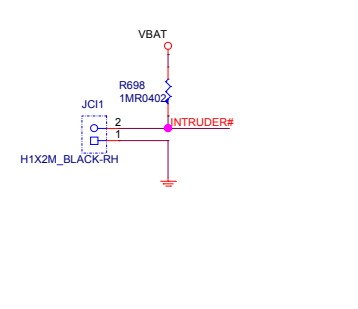




RTC



Chassis Intrusion



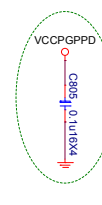
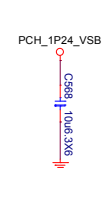
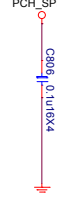
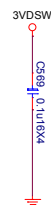
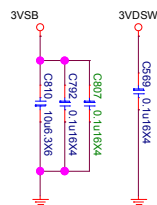
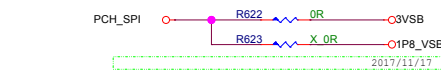
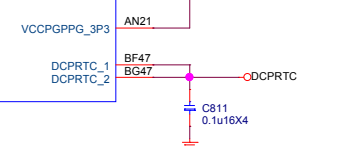
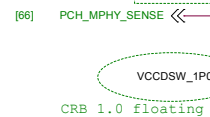
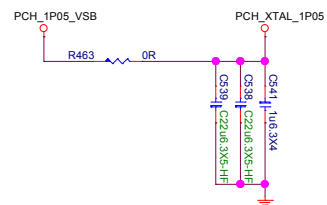










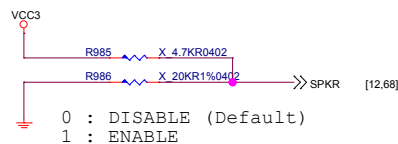


VSS

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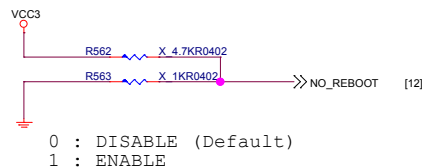


## TOP Swap



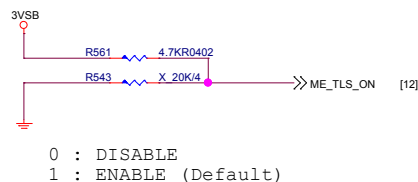
Internal pull-down is disabled after PCH\_PWROK is high.

## No Reboot



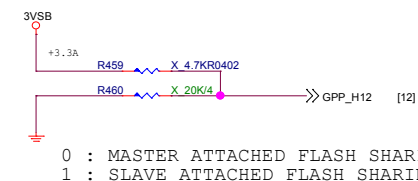
Internal pull-down is disabled after PCH\_PWROK is high.

## TLS confidentiality



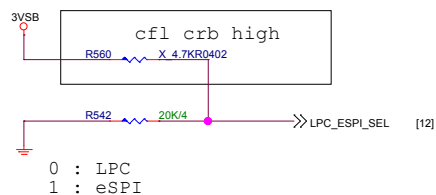
Internal pull-down is disabled after RSMRST# de-assert.

## ESPI FLASH SHARING MODE



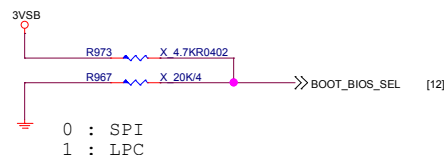
Internal pull-down is disabled after RSMRST# de-assert.

## LPC eSPI Mode



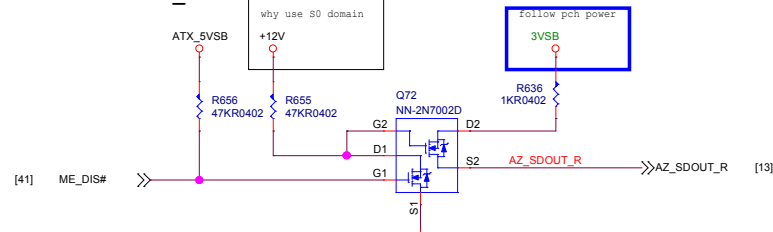
Internal pull-down is disabled after RSMRST# de-assert.

## Boot BIOS



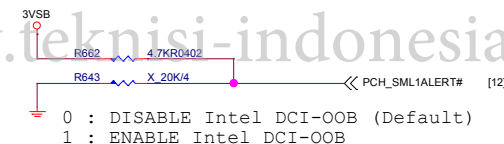
Internal pull-down is disabled after PCH\_PWROK is high.

## HDA\_SDO



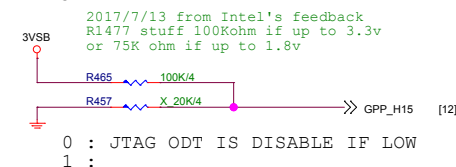
Internal pull-down is disabled after PCH\_PWROK is high.

## DCI ENABLE



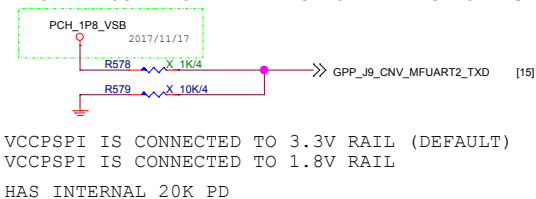
Internal pull-down is disabled after RSMRST# de-assert.

## ODT DISABLE

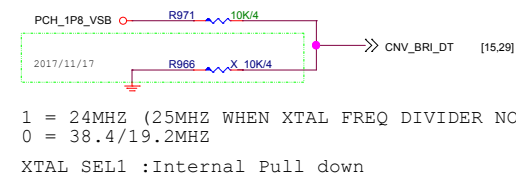


Internal pull-down is disabled after RSMRST# de-assert.

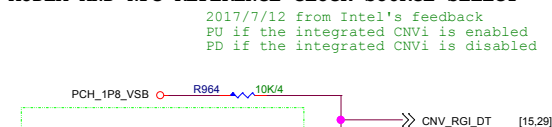
## SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE



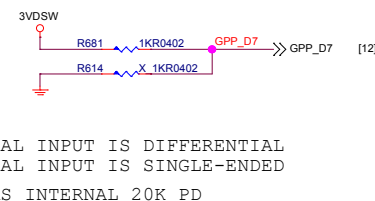
## XTAL FREQUENCY SELECTION



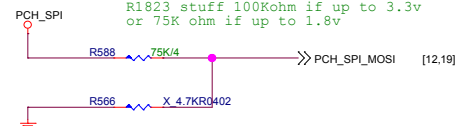
## MODEM AND NFC REFERENCE CLOCK SOURCE SELECT

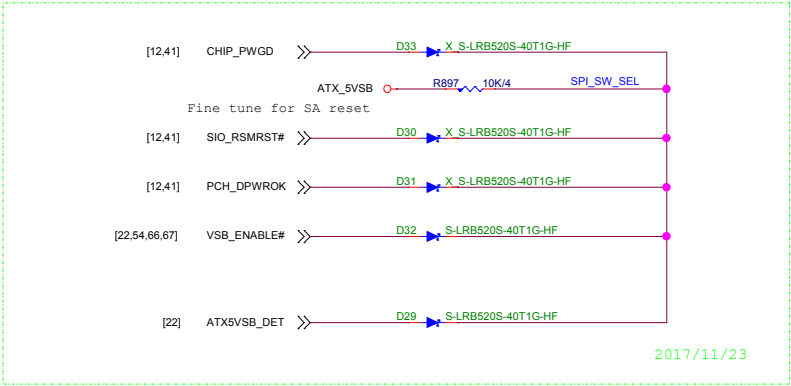
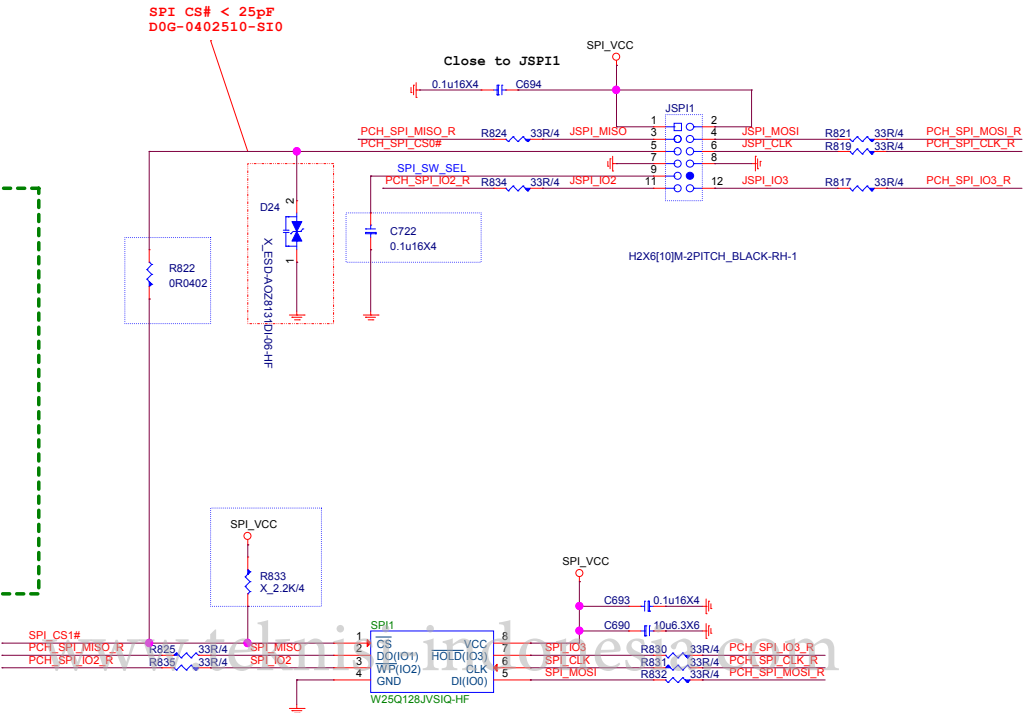
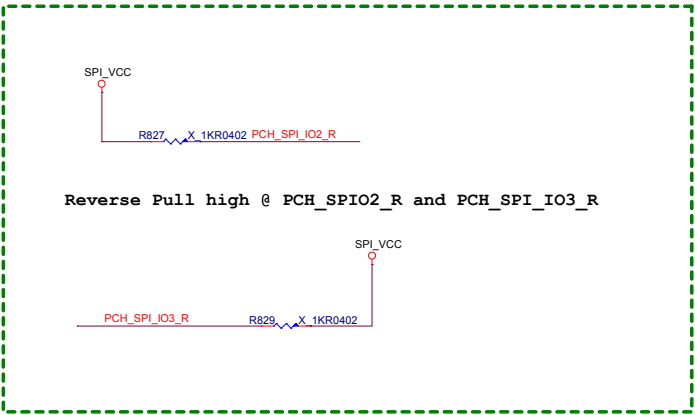
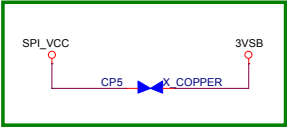
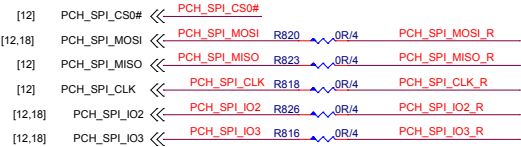


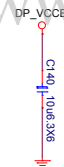
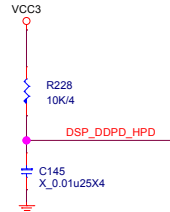
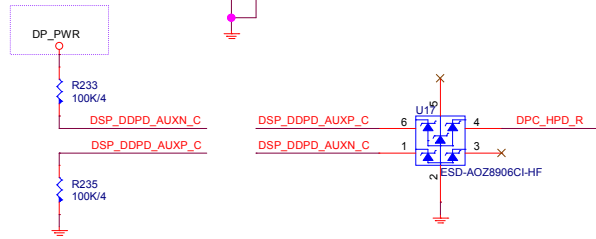
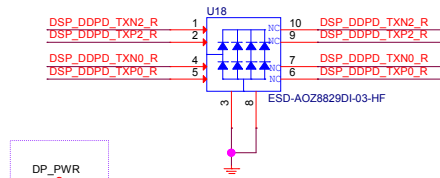
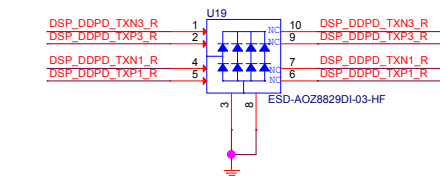
## XTAL INPUT MODE



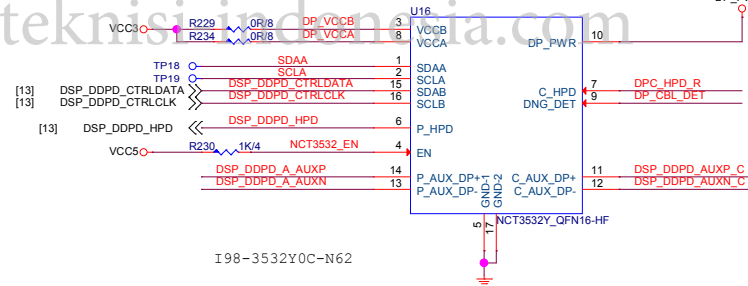
Reserved 2017/7/13 from Intel's feedback R1823 stuff 100Kohm if up to 3.3v or 75K ohm if up to 1.8v



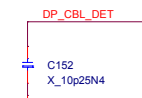
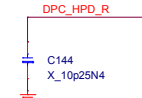
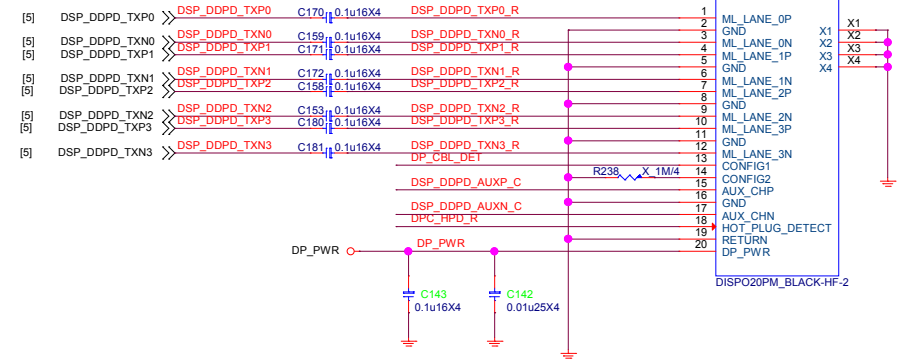




DP\_VCCB trace don't less than 30 mil

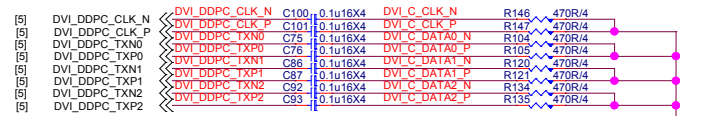


DP

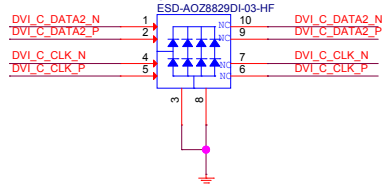




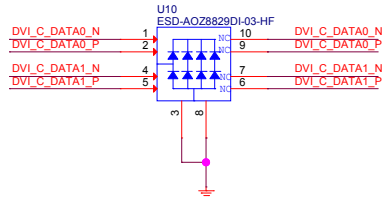
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



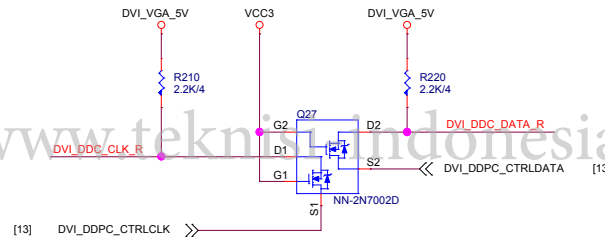
U26 AVL:D0G-05A050C-005  
D0G-06A050C-A68



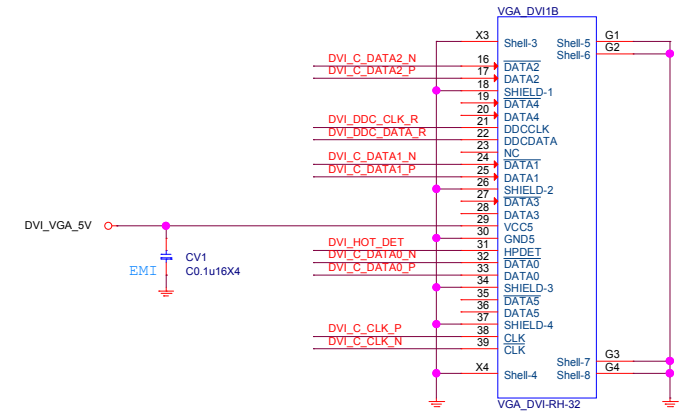
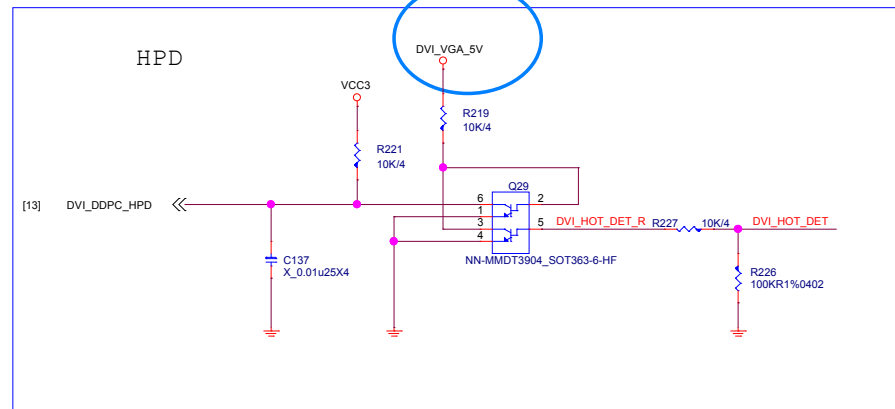
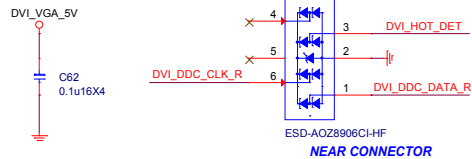
U27 AVL:D0G-05A050C-005  
D0G-06A050C-A68



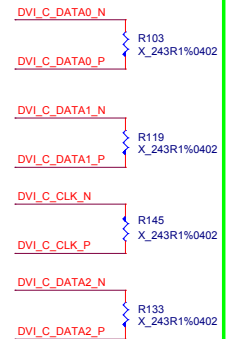
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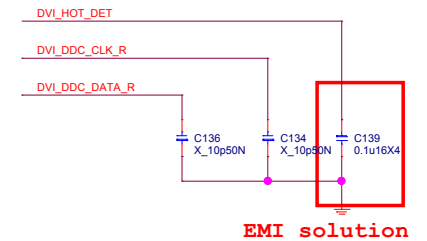
EMI Cap near connector DVI1



For EMI

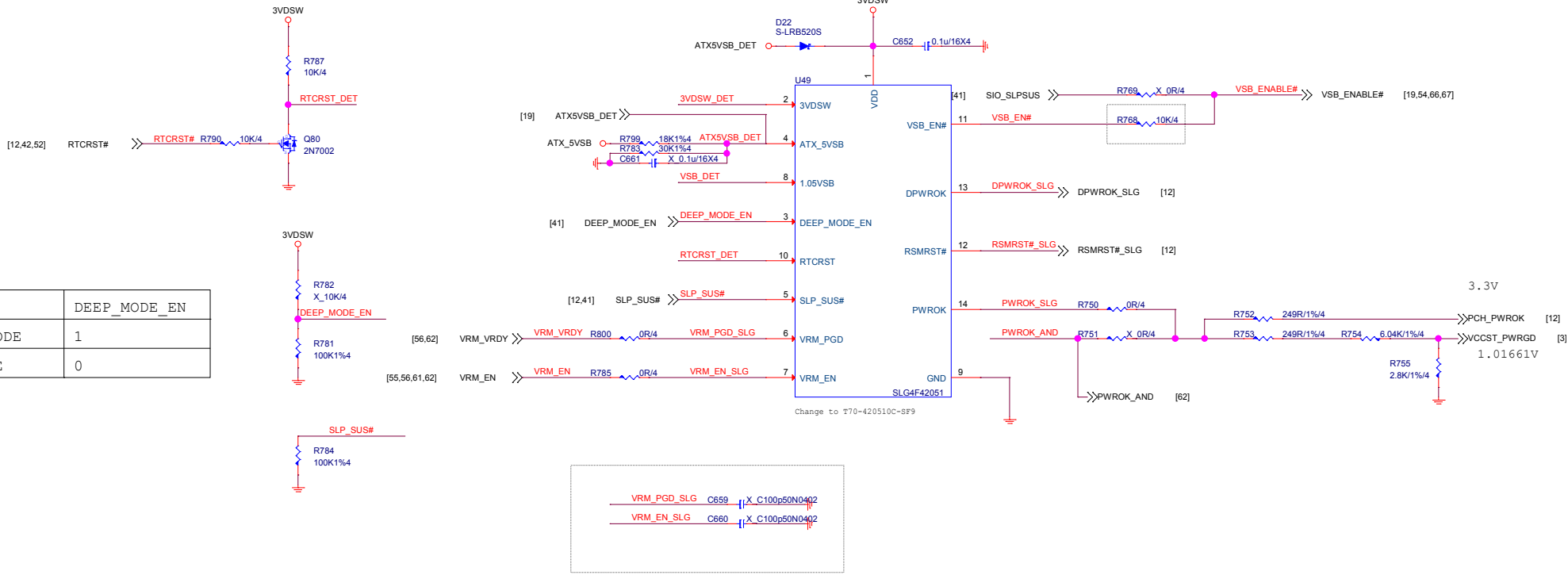


EMI

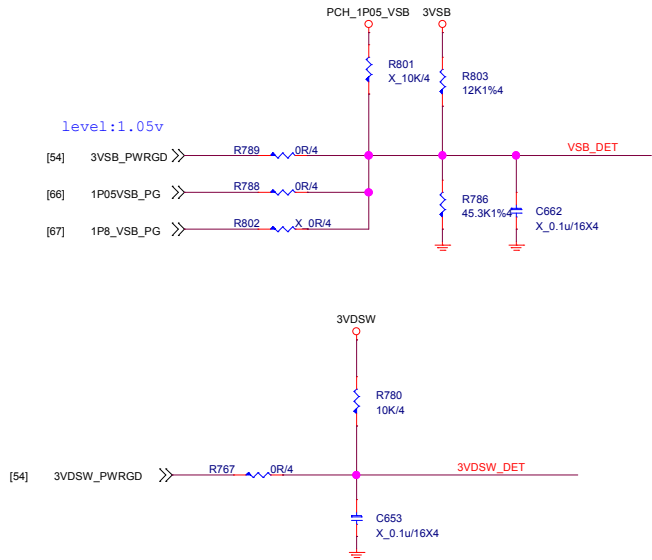


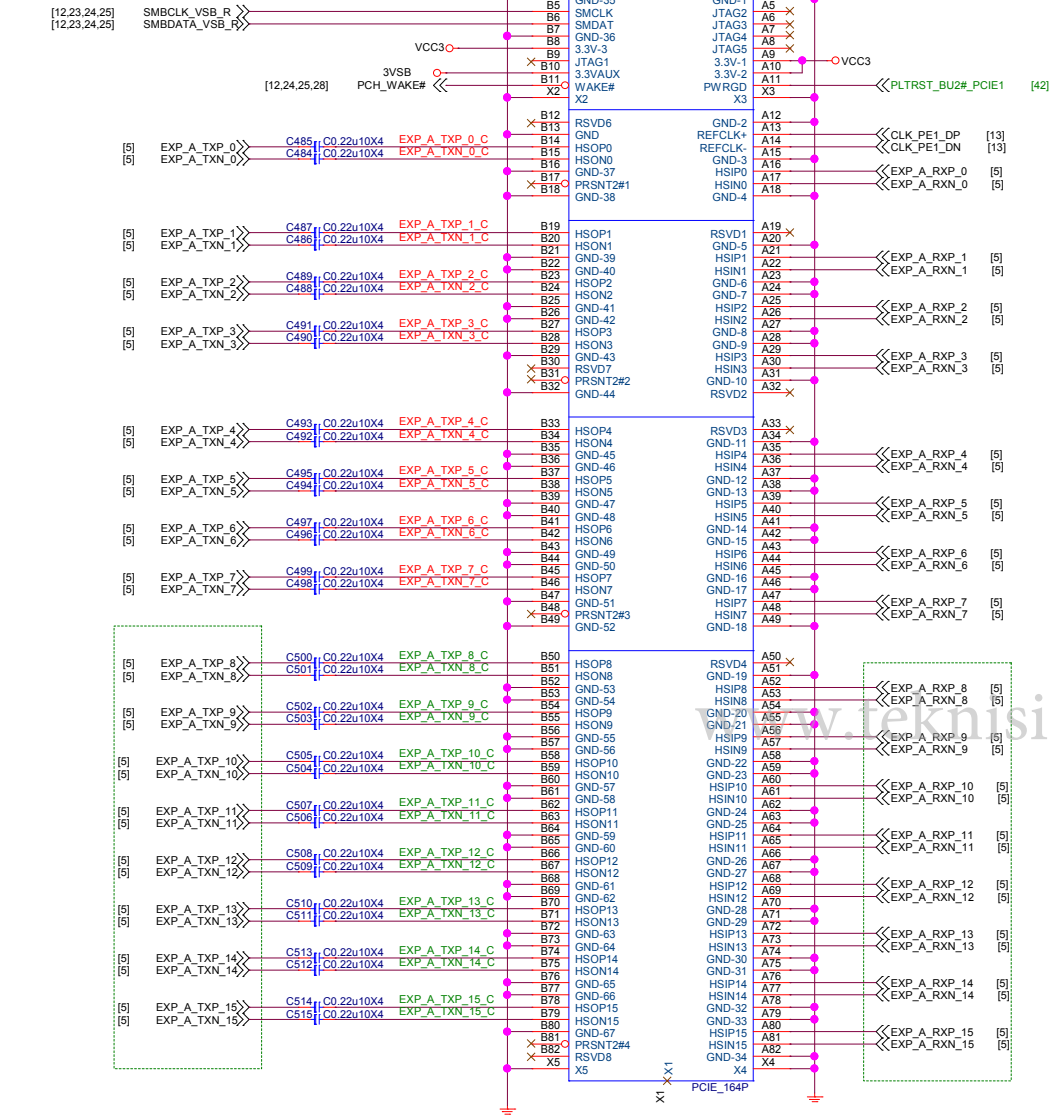
msi MICRO-STAR INT'L CO.,LTD.

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

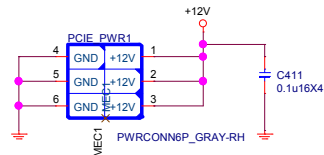
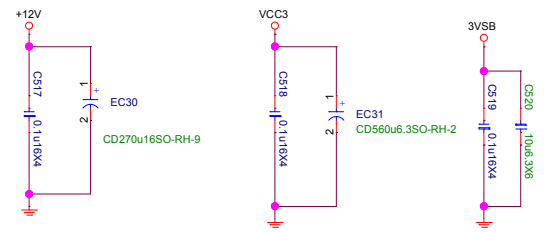
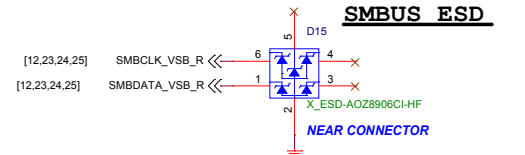


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5.5A at +12V  
3A at VCC3  
375mA at 3VSB

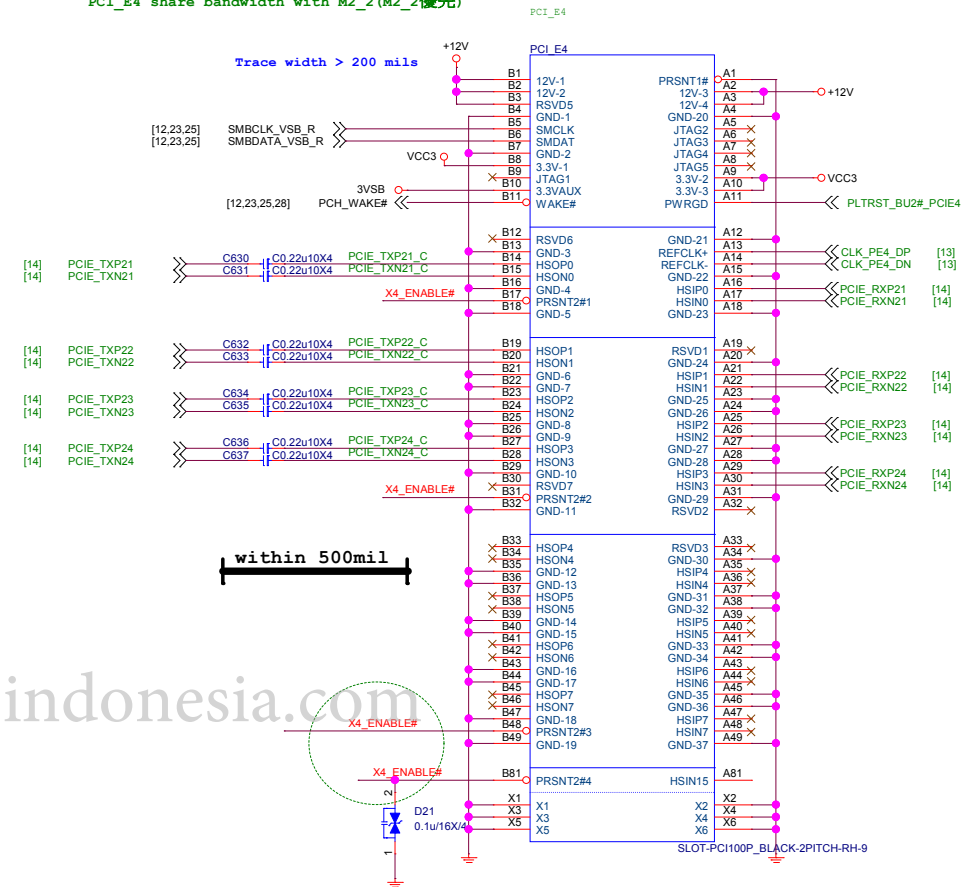


N93-06M0261-H06

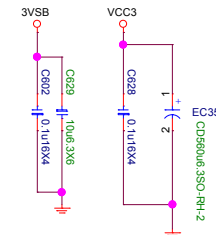
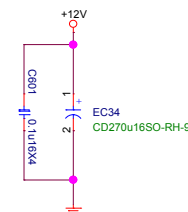
# PCI Express X4 Slot

2.1A at +12V  
3A at VCC3  
375mA at 3VSB

PCI\_E4 share bandwidth with M2\_2(M2\_2優先)

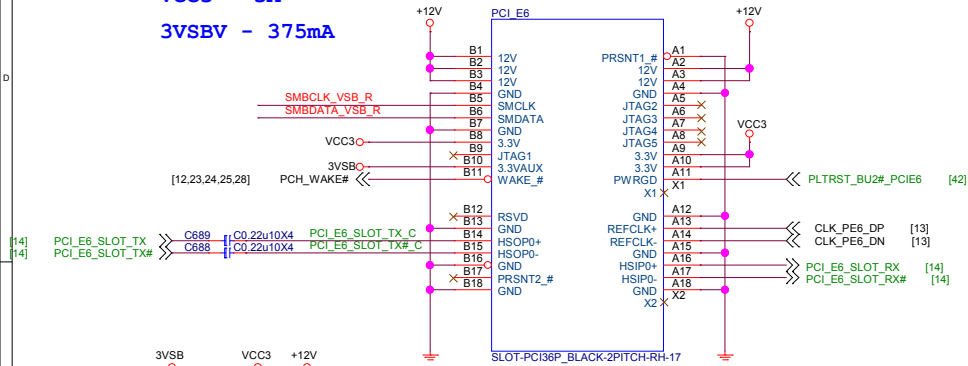


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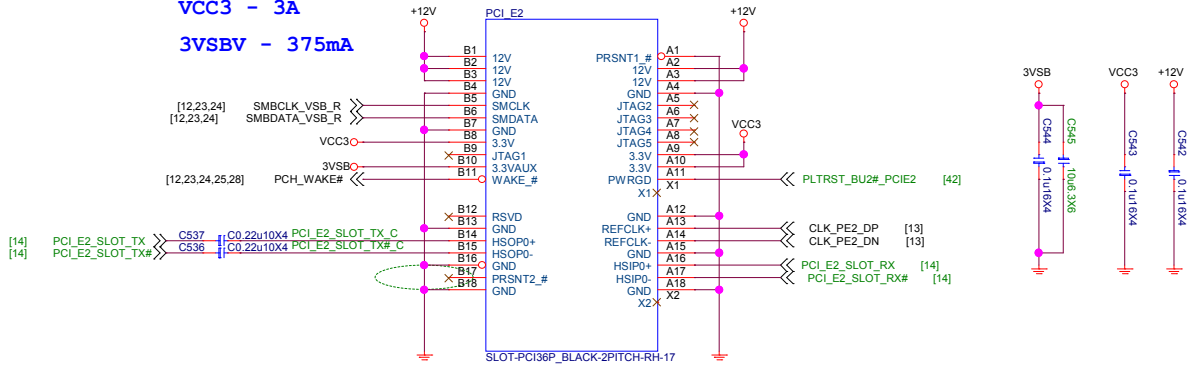


PCH PCIE X1 Slot

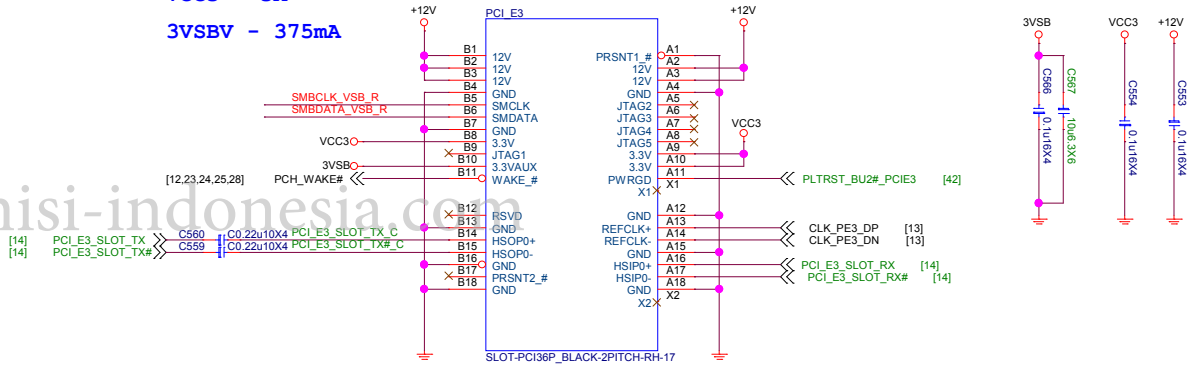
12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



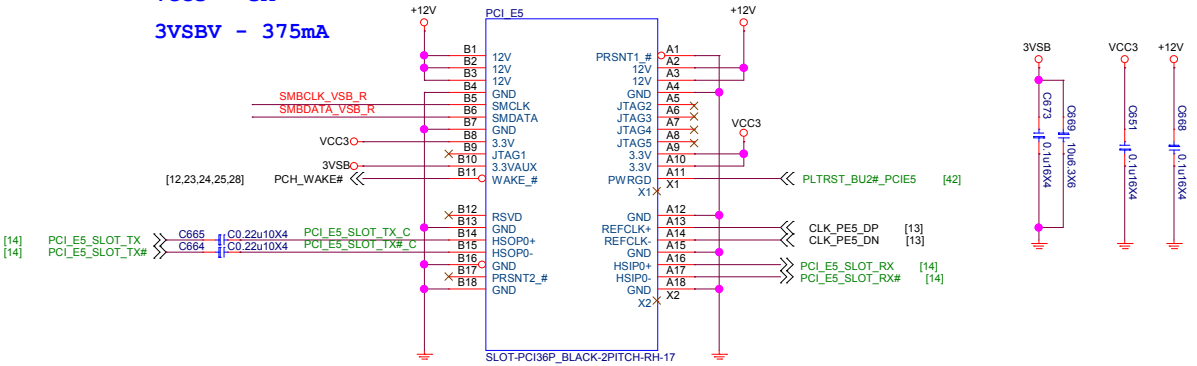
12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



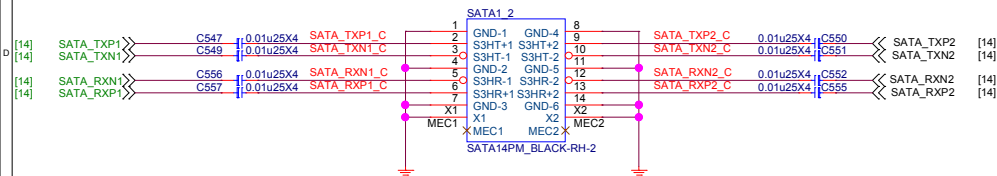
12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



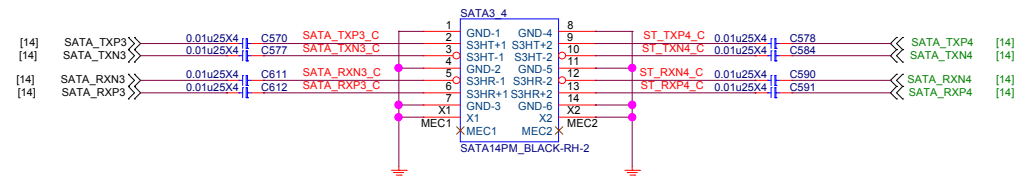
12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



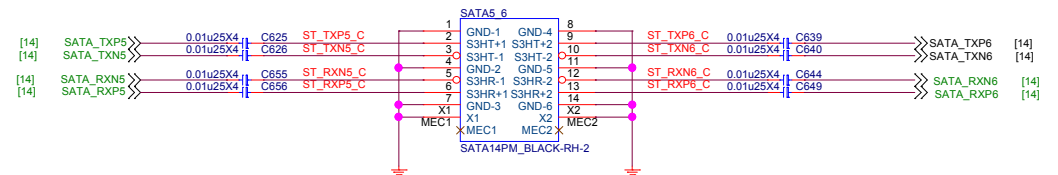
SATA 6G PORT 1.2



SATA 6G PORT 3.4



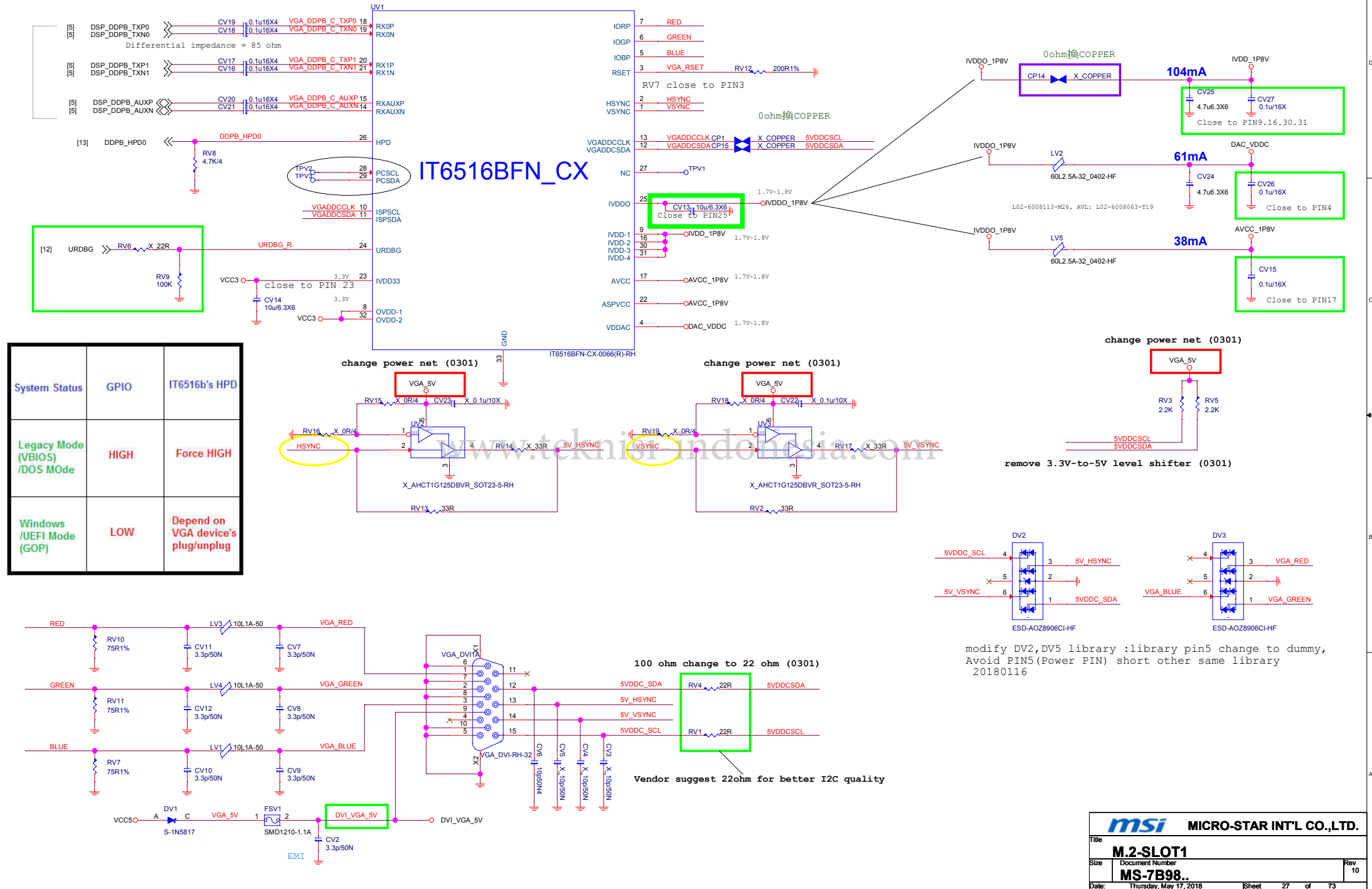
SATA 6G PORT 5.6

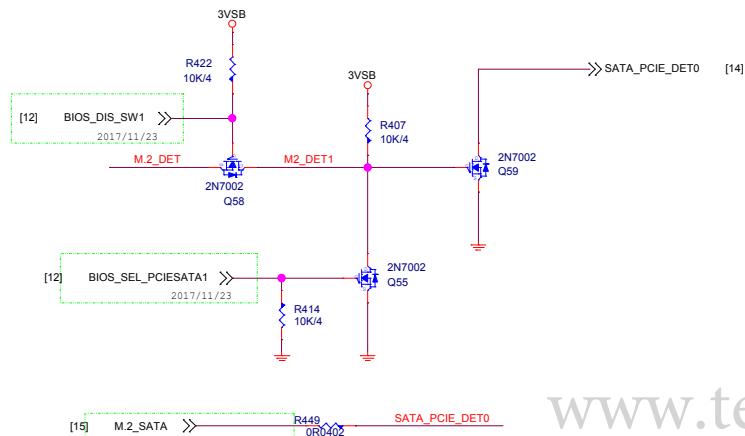


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**Note:**  
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



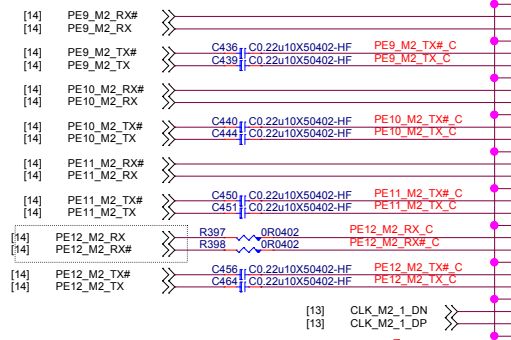


# BIOS\_MODE

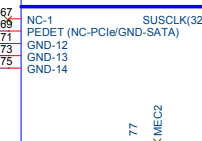
DIS_SW	M1_SEL_PCIESATA	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

SATA 要反接

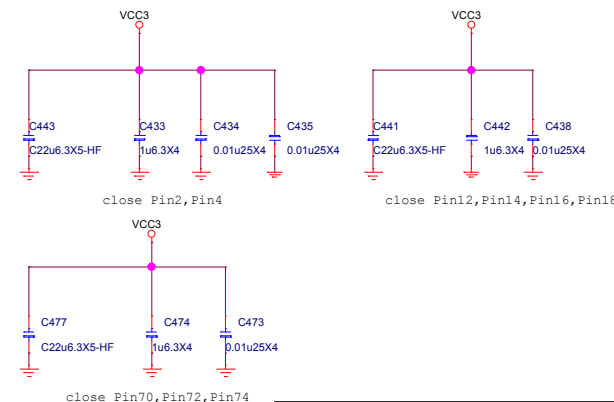
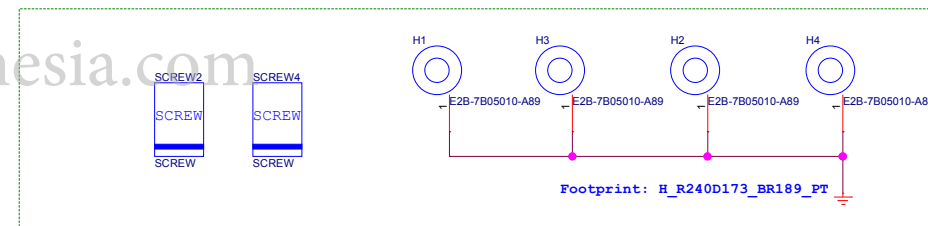
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## KEY M

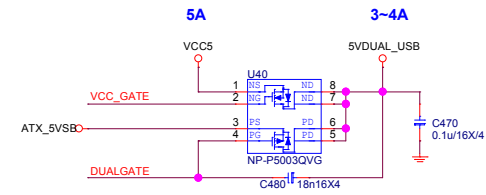
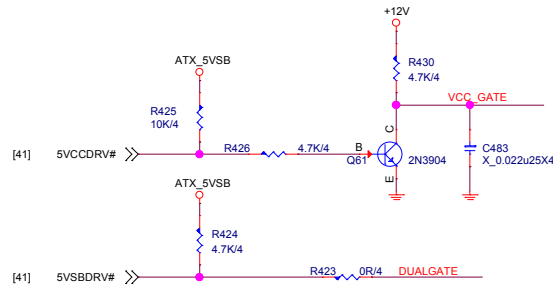


D20,D21 Close to M2 connector

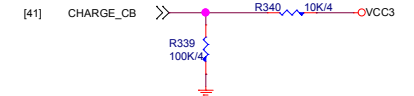




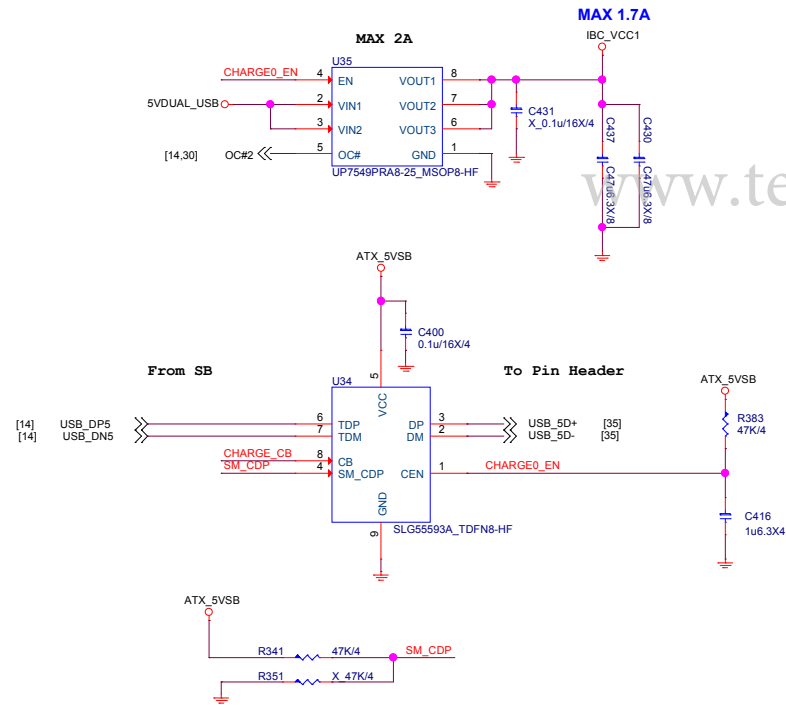
## 5VDUAL\_USB



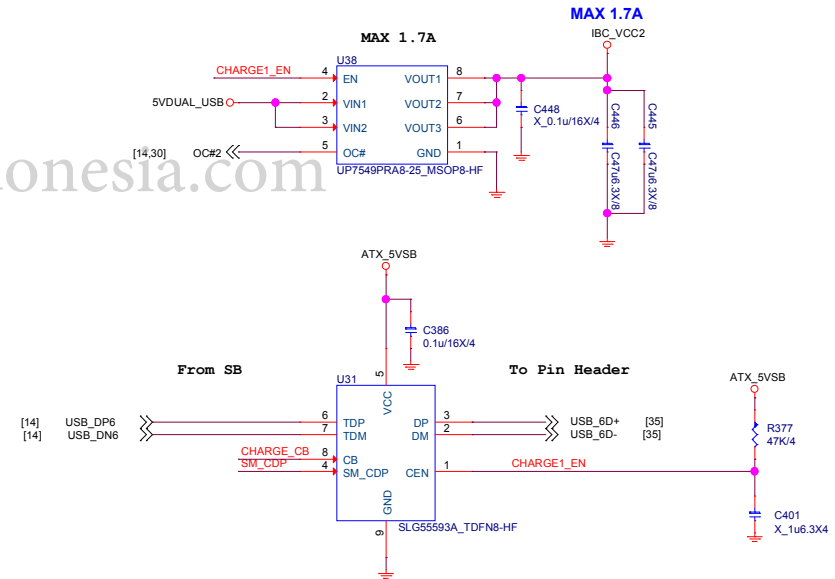
Pin power : I\_3VSB  
Register power : I\_3VSB  
Register reset : I\_3VSB



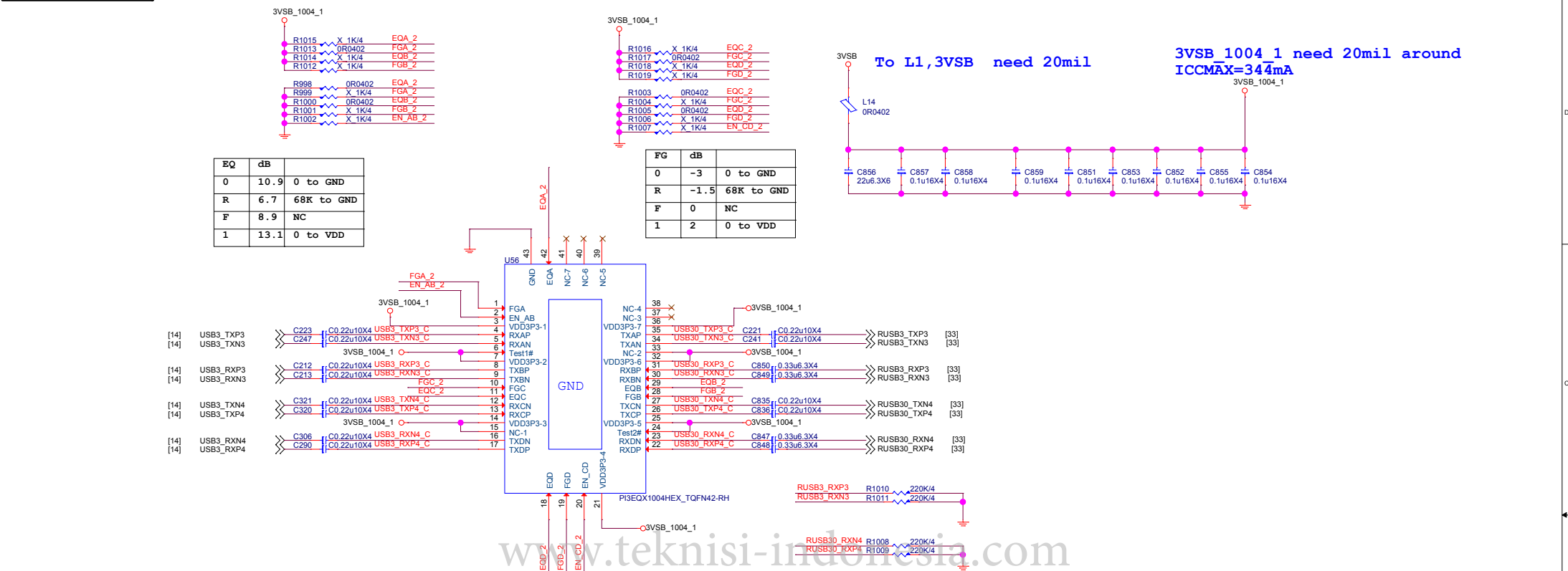
## USB POWER PORT 0 For USB Charging



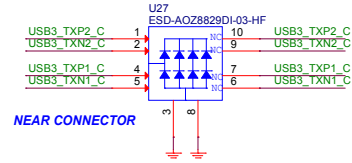
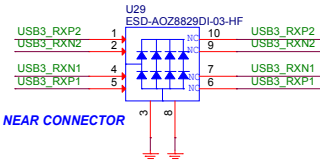
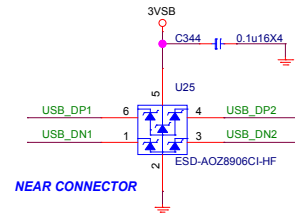
## USB POWER PORT 1 For USB Charging



Rear USB3.1 Redriver

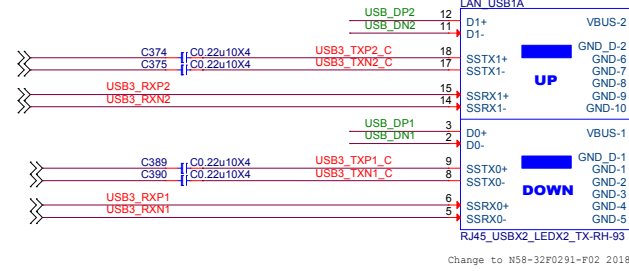


[14] USB\_DP2  
[14] USB\_DN2  
[14] USB\_DP1  
[14] USB\_DN1



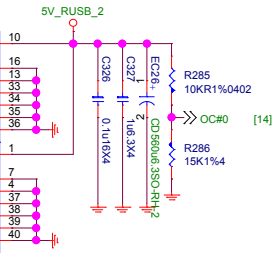
[14] USB3\_TXP2  
[14] USB3\_TXN2  
[14] USB3\_RXP2  
[14] USB3\_RXN2

[14] USB3\_TXP1  
[14] USB3\_TXN1  
[14] USB3\_RXP1  
[14] USB3\_RXN1



2017/6/22  
EC58 is changed from 470uF  
to 560uF by buyer request

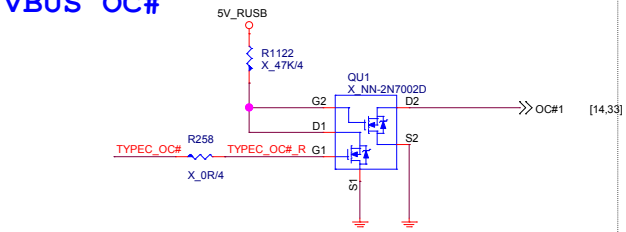
### LAN USB1



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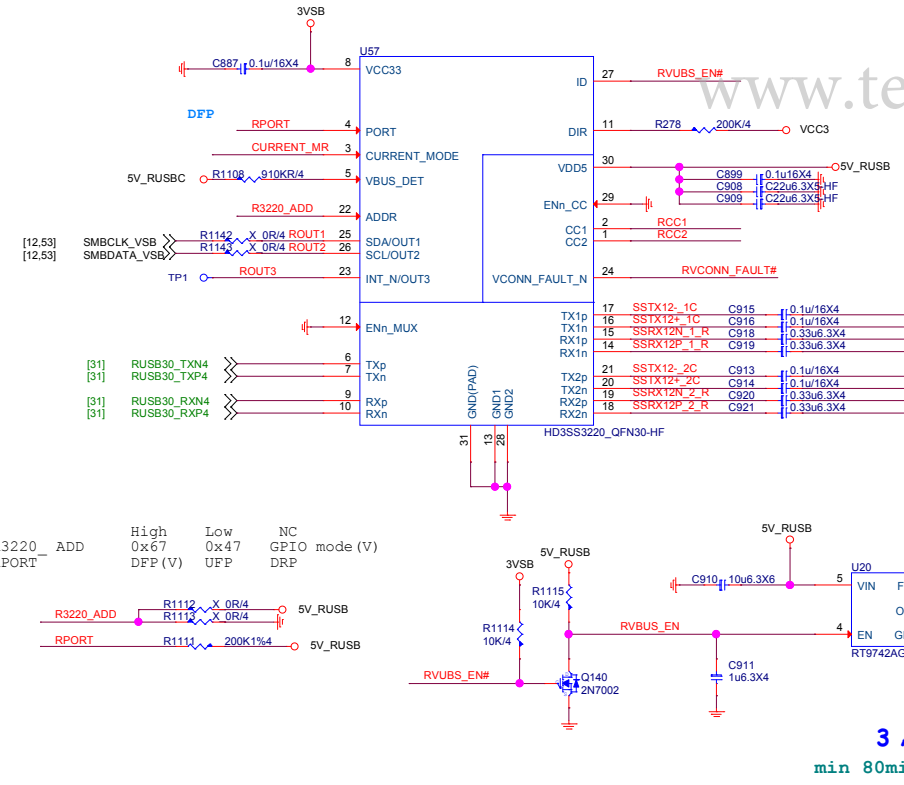
VBUS OC#



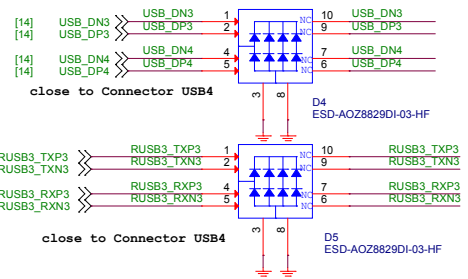
VCONN OC#



USB Type-C MUX with Configuration Channel (CC)



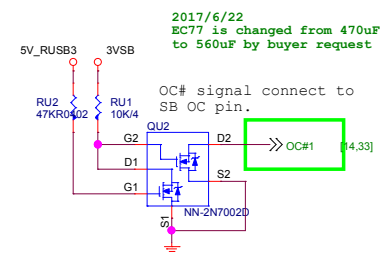
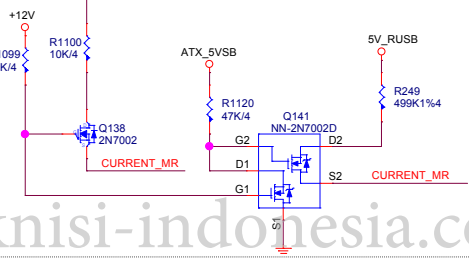
3 A  
min 80mil.



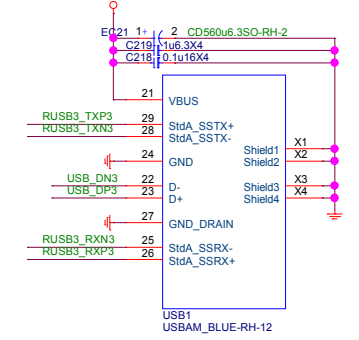
Current Mode

3A under S0 mode  
1.5A under S3 mode

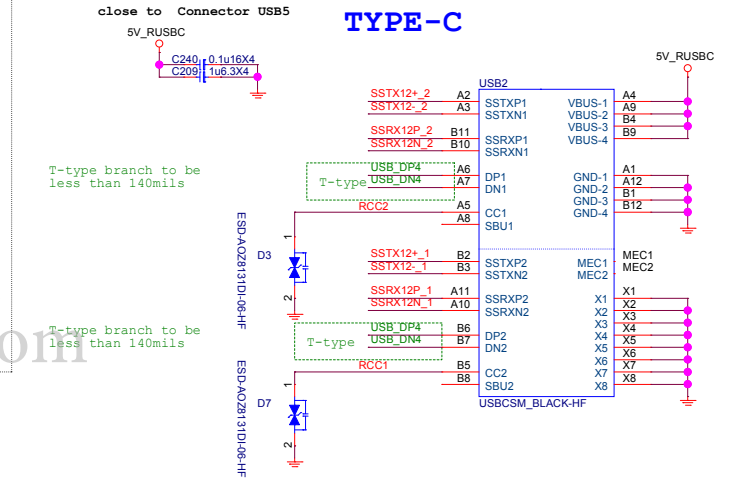
L - Default for 900mA  
M - Mid (500K) for 1.5A  
H - High (10K) for 3A



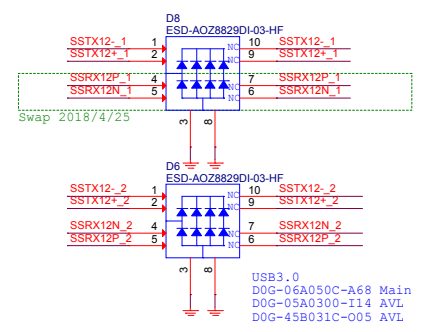
TYPE-A



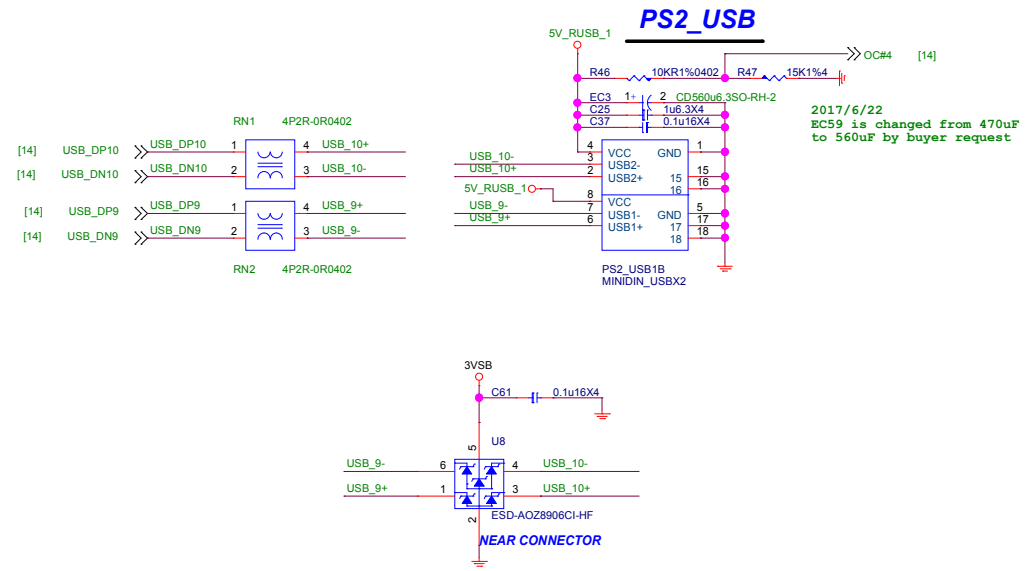
TYPE-C



ESD Protection NEAR AC CAP



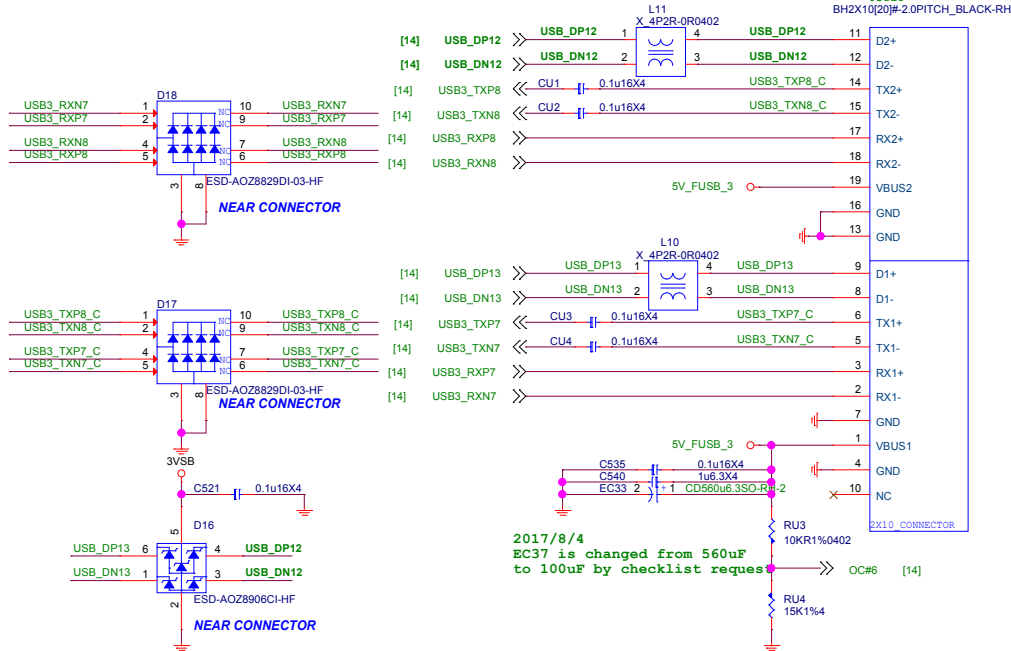
REAR USB2.0



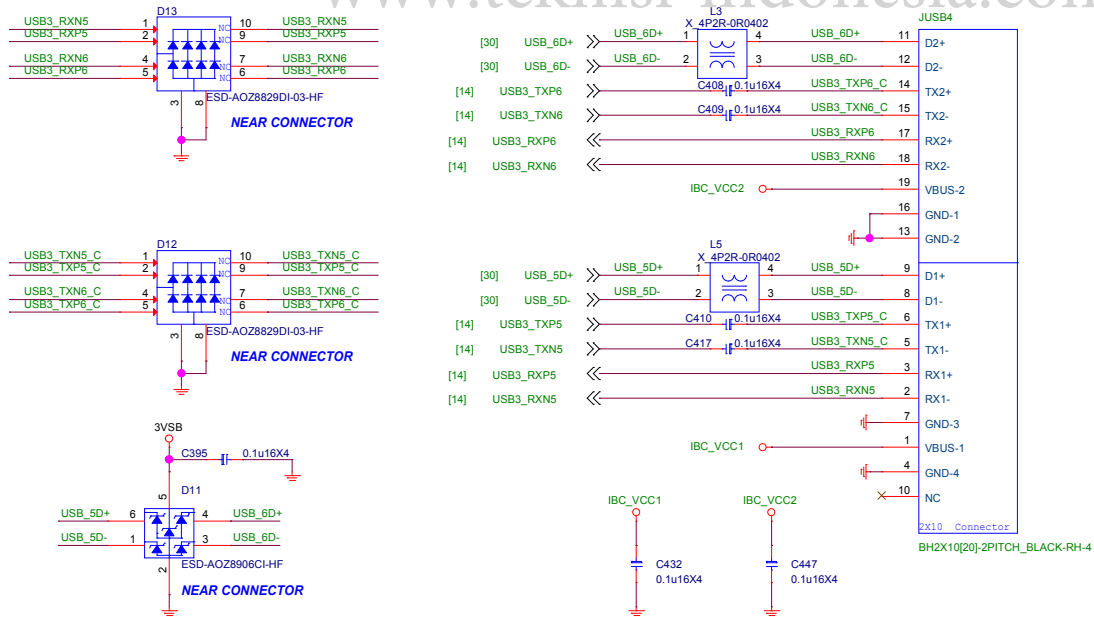
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FUSB5 90°

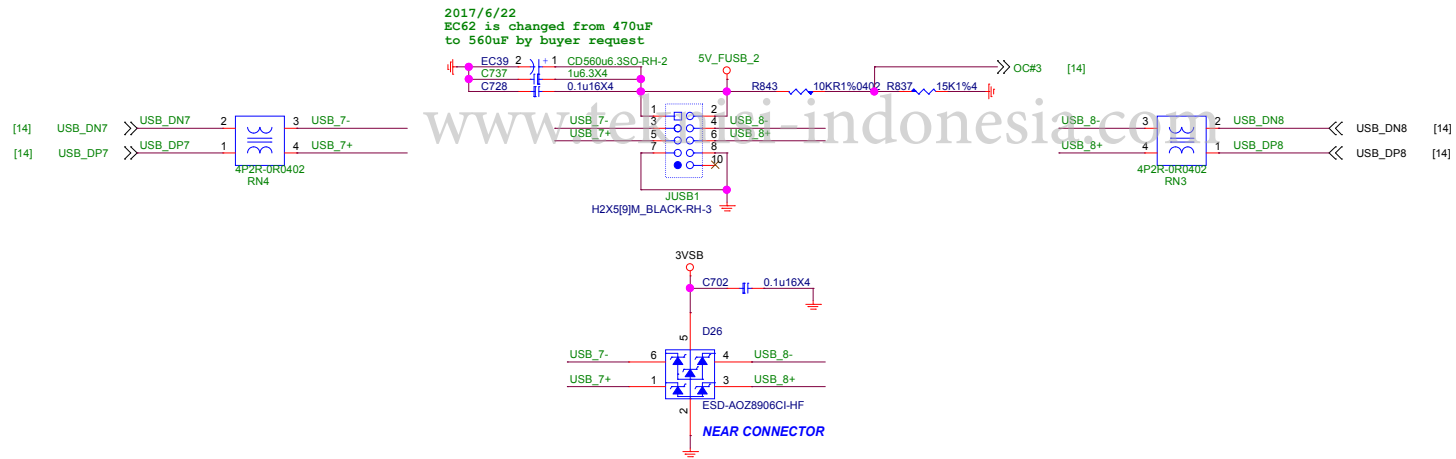
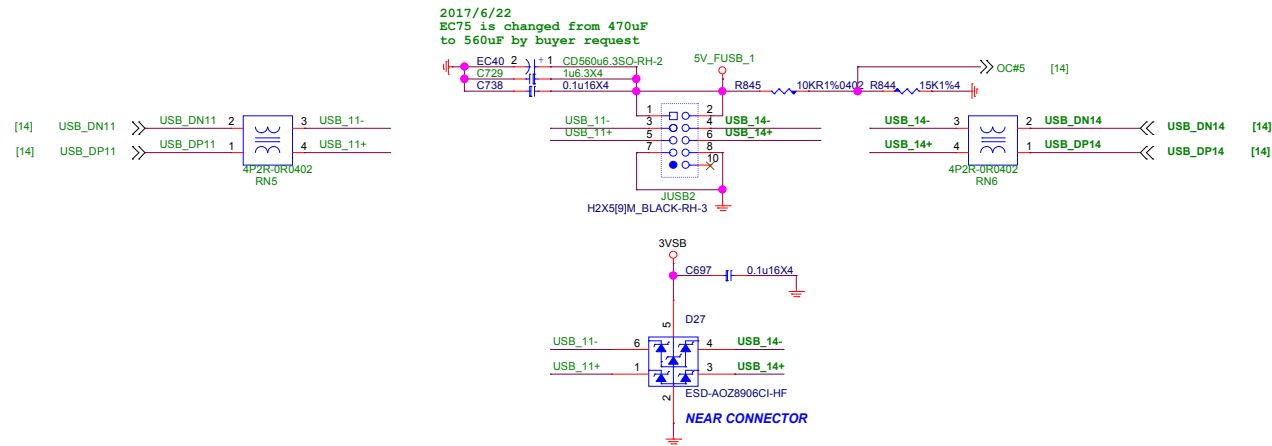
B SKU 不上件



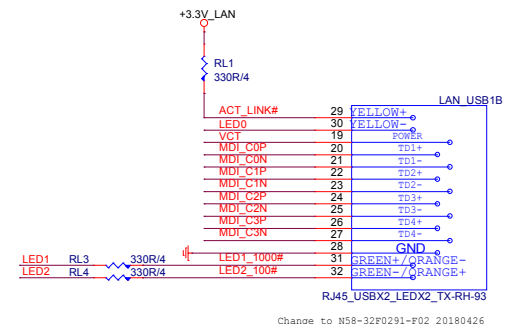
FUSB3 180°



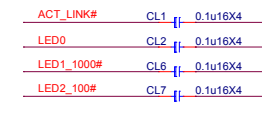
# FRONT USB2.0



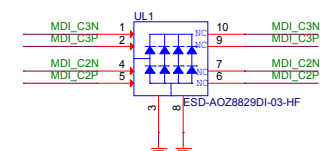
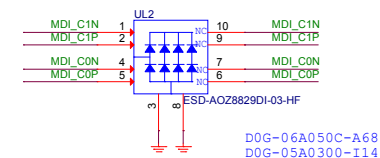
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For EMI



UL2&UL3 close to connector

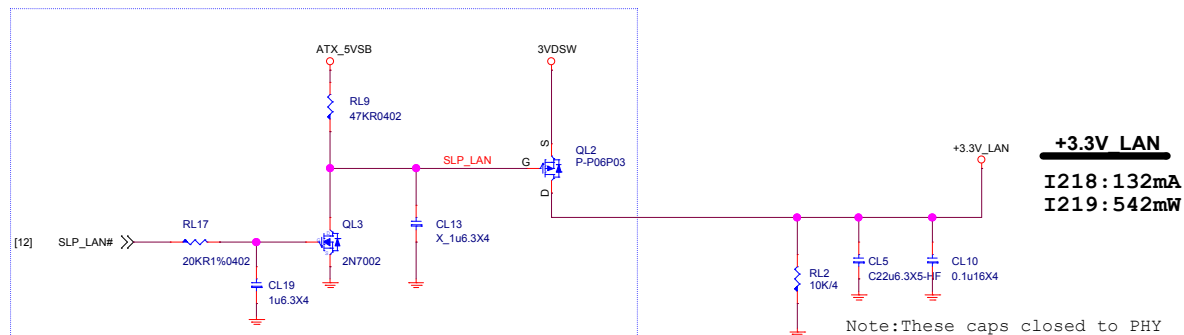


LAN DISABLE# must be connected to  
CHT's LAN PHY PWR CTRL

PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port.  
If CLK REQ N is not used, pin48 is pulled up 10K $\Omega$  to 3.3V LAN

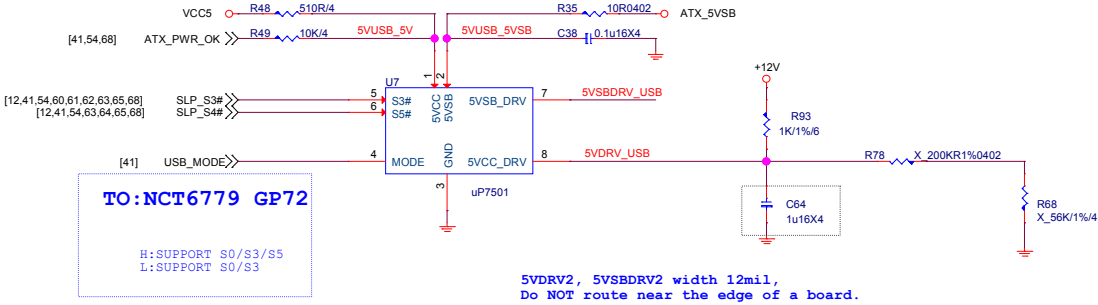
The 10Kohm pull-up resistor (RL18) of CLK\_REQ\_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:  
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

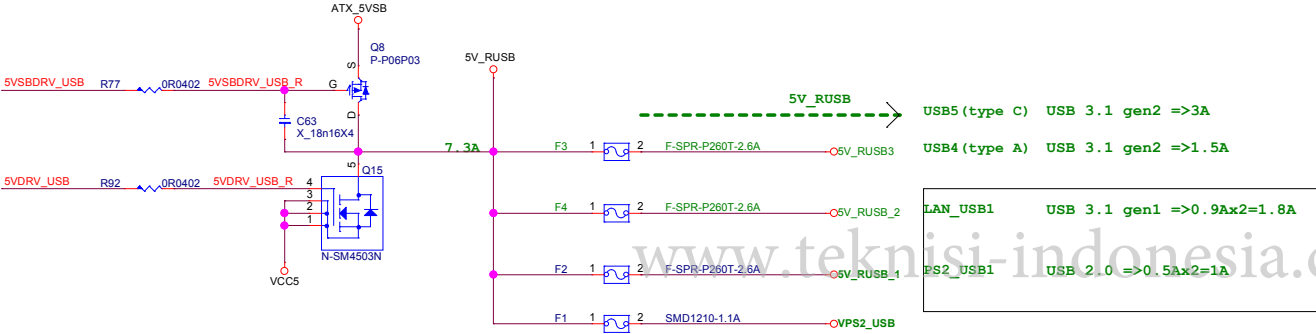


Note: These caps closed to PHY

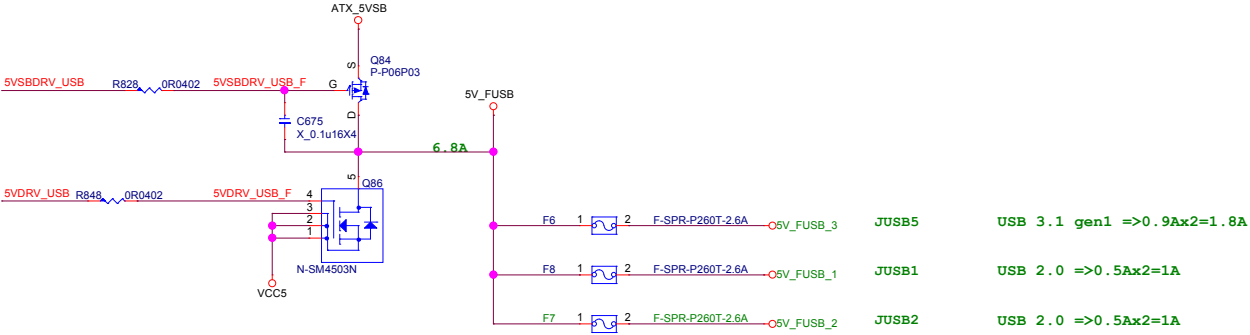
USB POWER



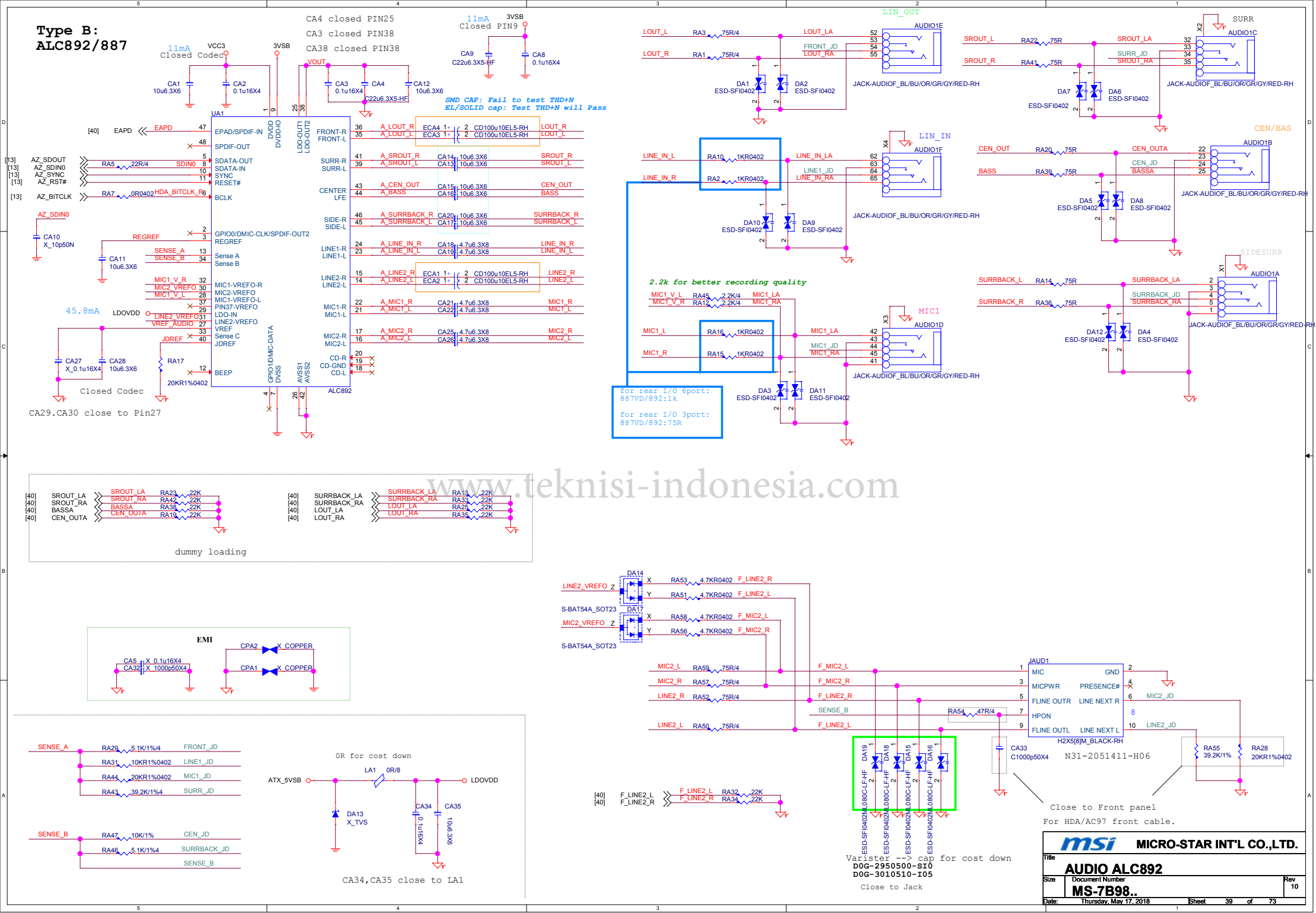
REAR USB PORT POWER



FRONT USB PORT POWER



# Type B: ALC892/887



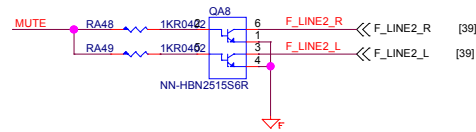


De-pop circuit for Rear Line out & Front Headphone out)

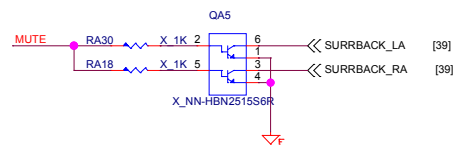
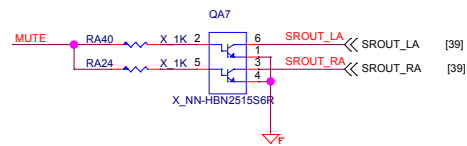
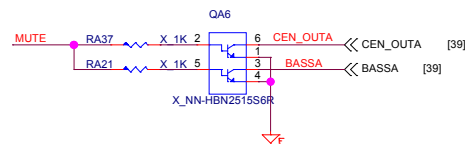
*De-pop circuit for Real Line out & Front Headphone out)*

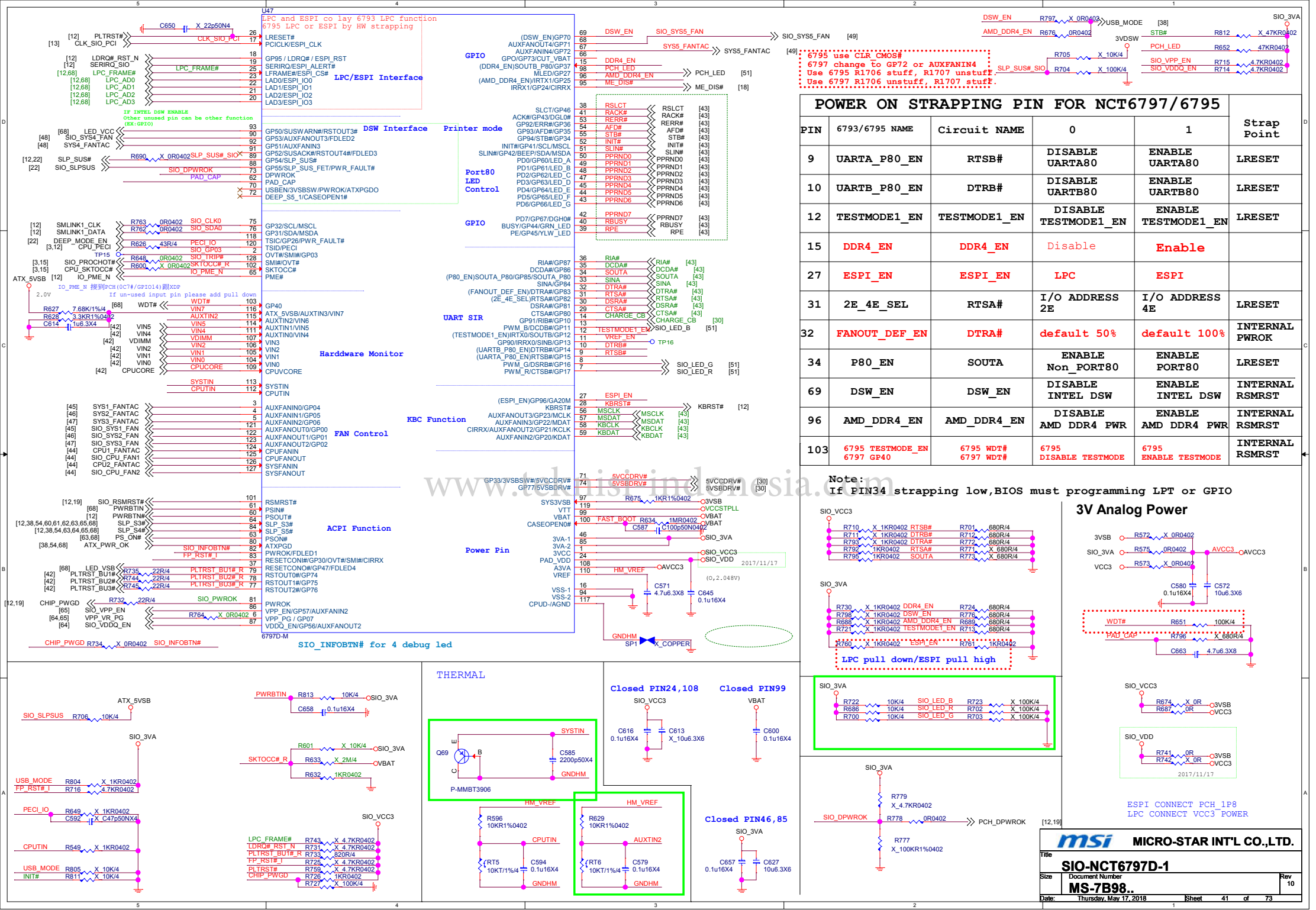
Digital

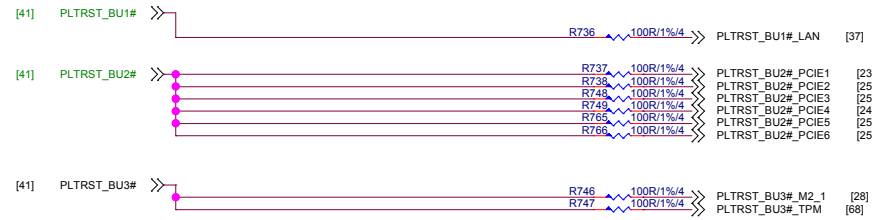
[39] EAPD >> EAPD RA26 1KR0402 EAPD\_R B QA3 P-MMBT3906 VCC3 RA9 10K/4 B QA1 P-MMBT3906 RA8 0R0402 RA4 10K/4 B RA6 220K/4 3VSB CA6 0.1u16X4 CA7 C22u6.3X5-HF MUTE



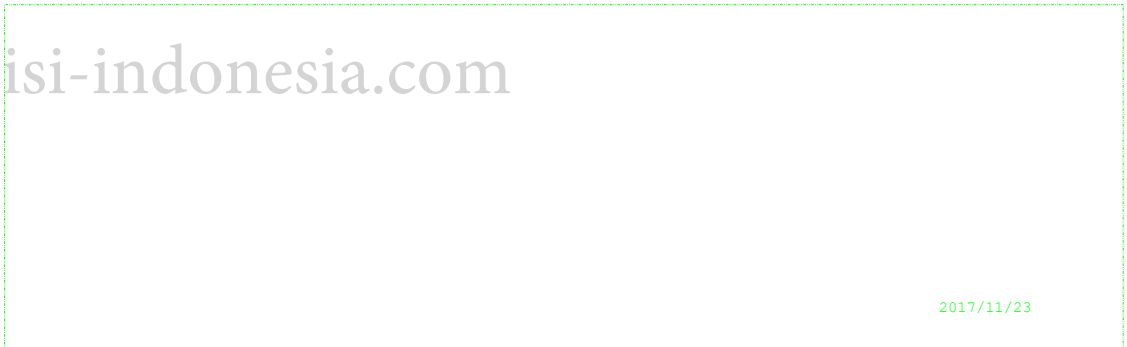
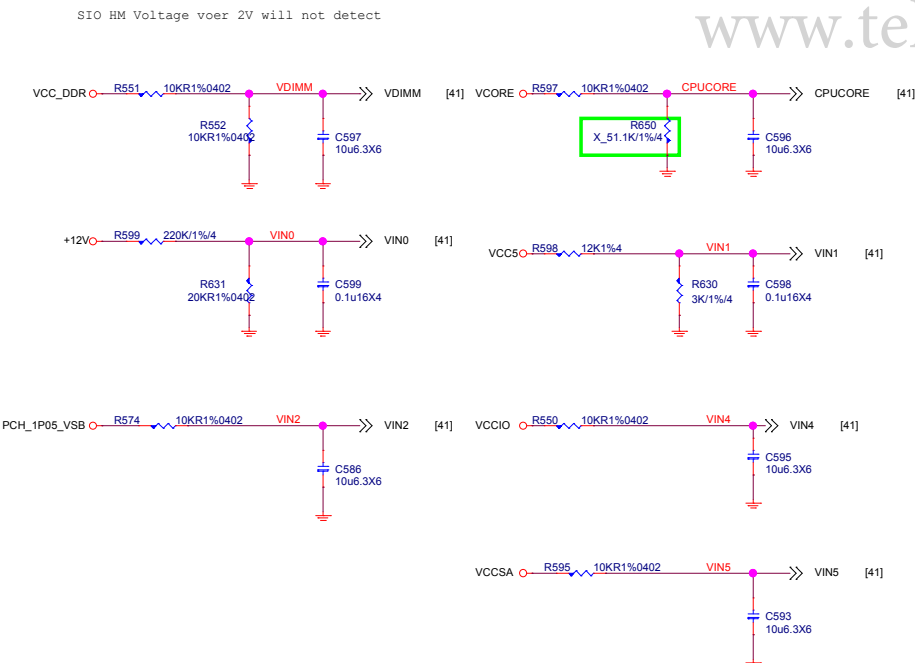
(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change CA5, CA11, CA12, CA13, CA21, CA22 to TVS)



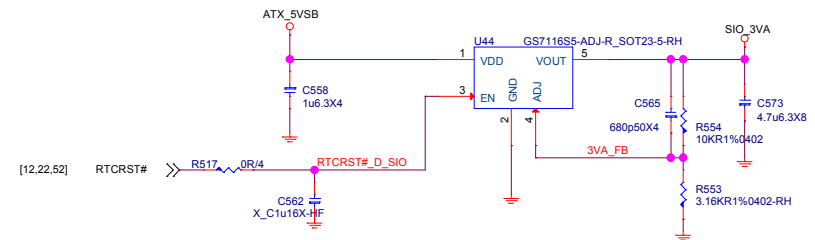




# HW Monitor - Voltage



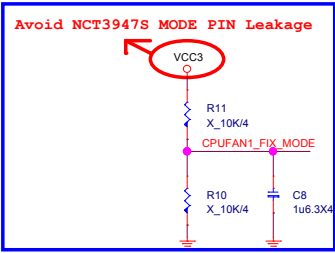
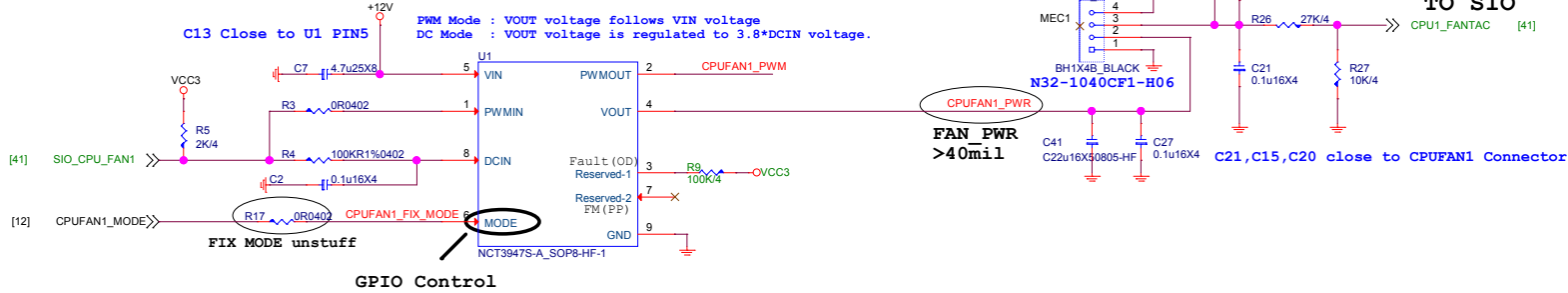
2017/11/23





TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

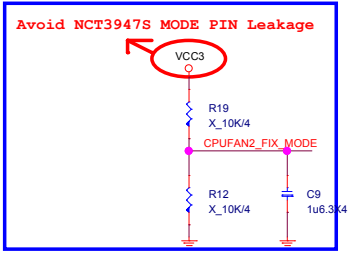
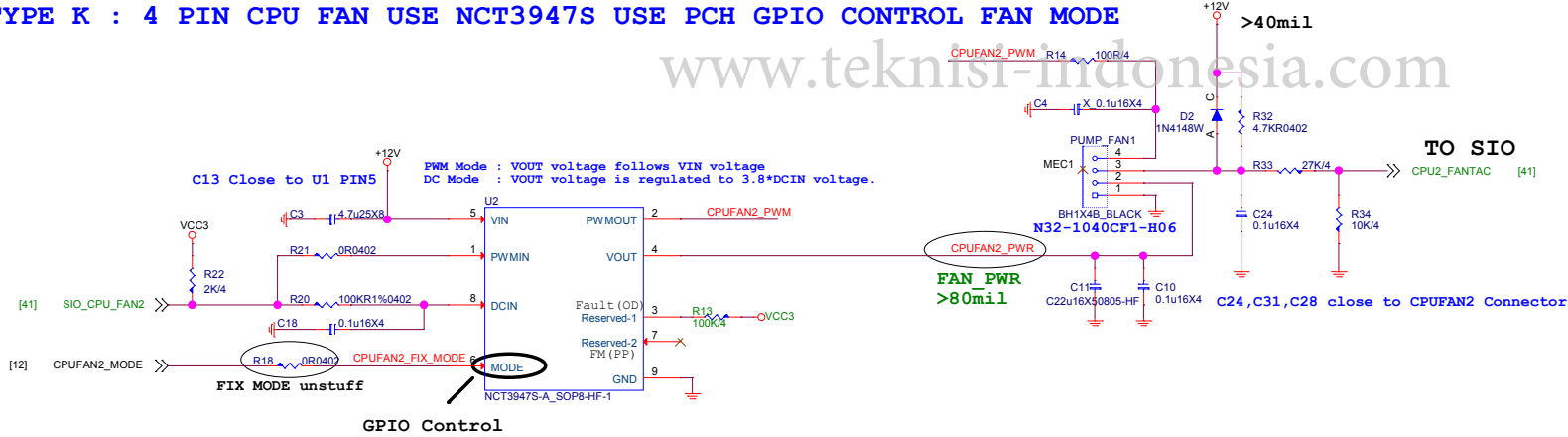
- 1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
- 2. GPIO可以由BIOS切換 PWM/DC MODE
- 3. OCF拉回GPIO給BIOS認
- 4. PWM OR DC FAN拉回GPIO給BIOS認
- 5. FAN轉速加快的時候由SOFTWARE 控制GPIO讓燈的變化



Resever For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

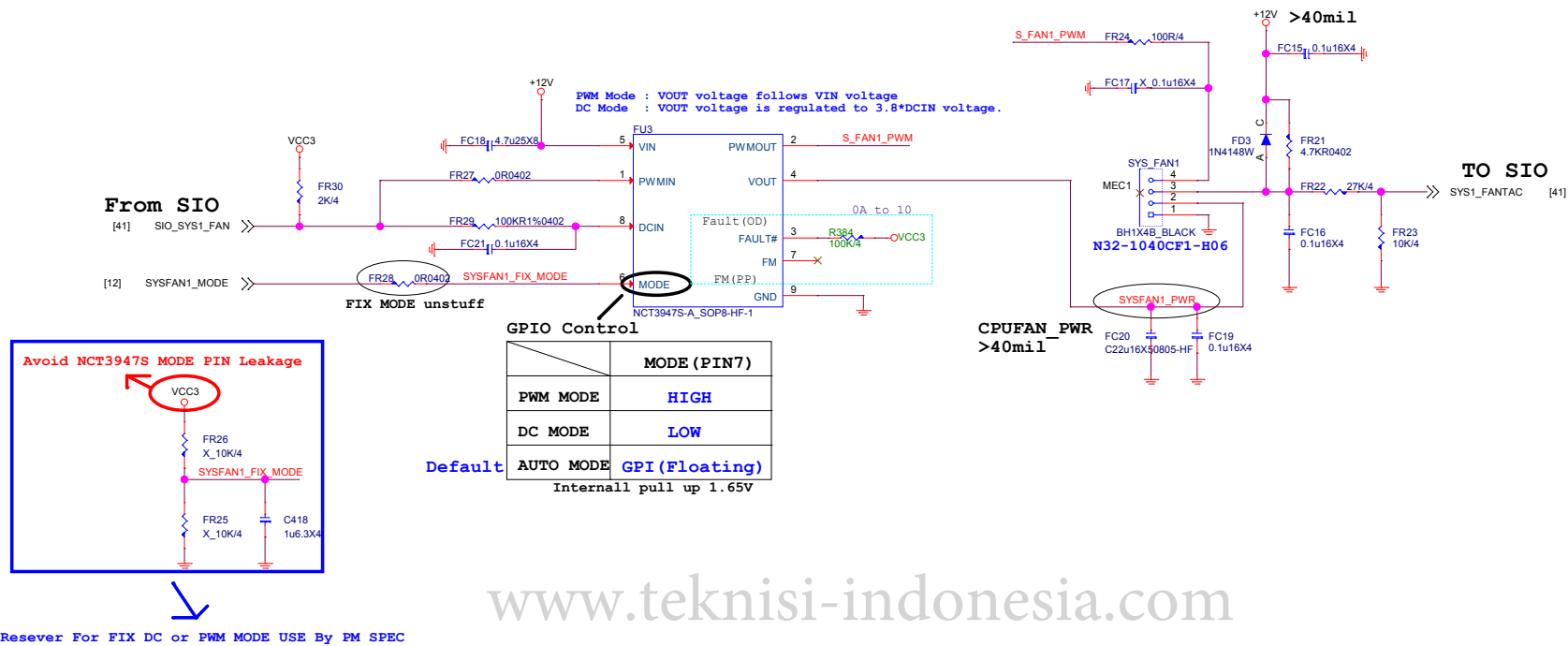
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Resever For FIX DC or PWM MODE USE By PM SPEC

- 1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
- 2. FAULT : USE FAULT PIN Triger OVT/OCF Protection, LOW Atcive (Reserve NEW IC)
- 3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

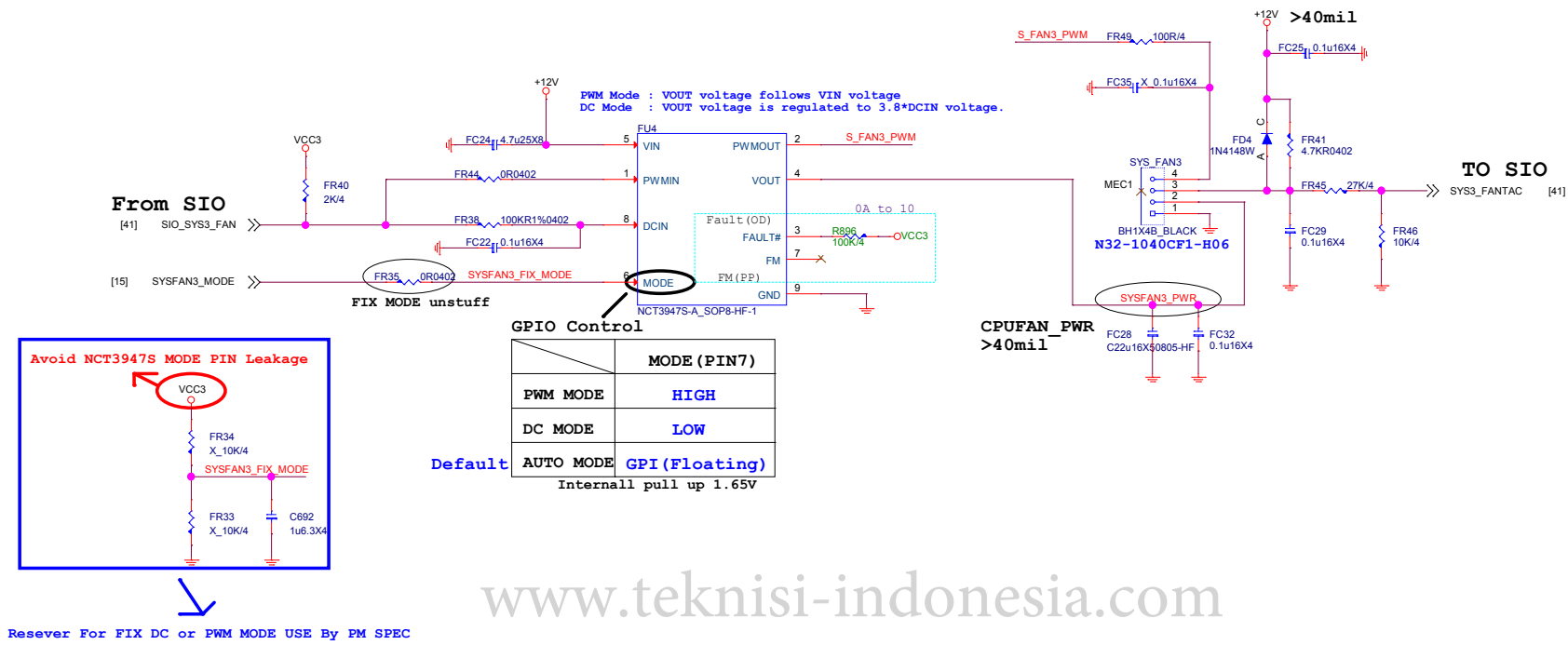
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE





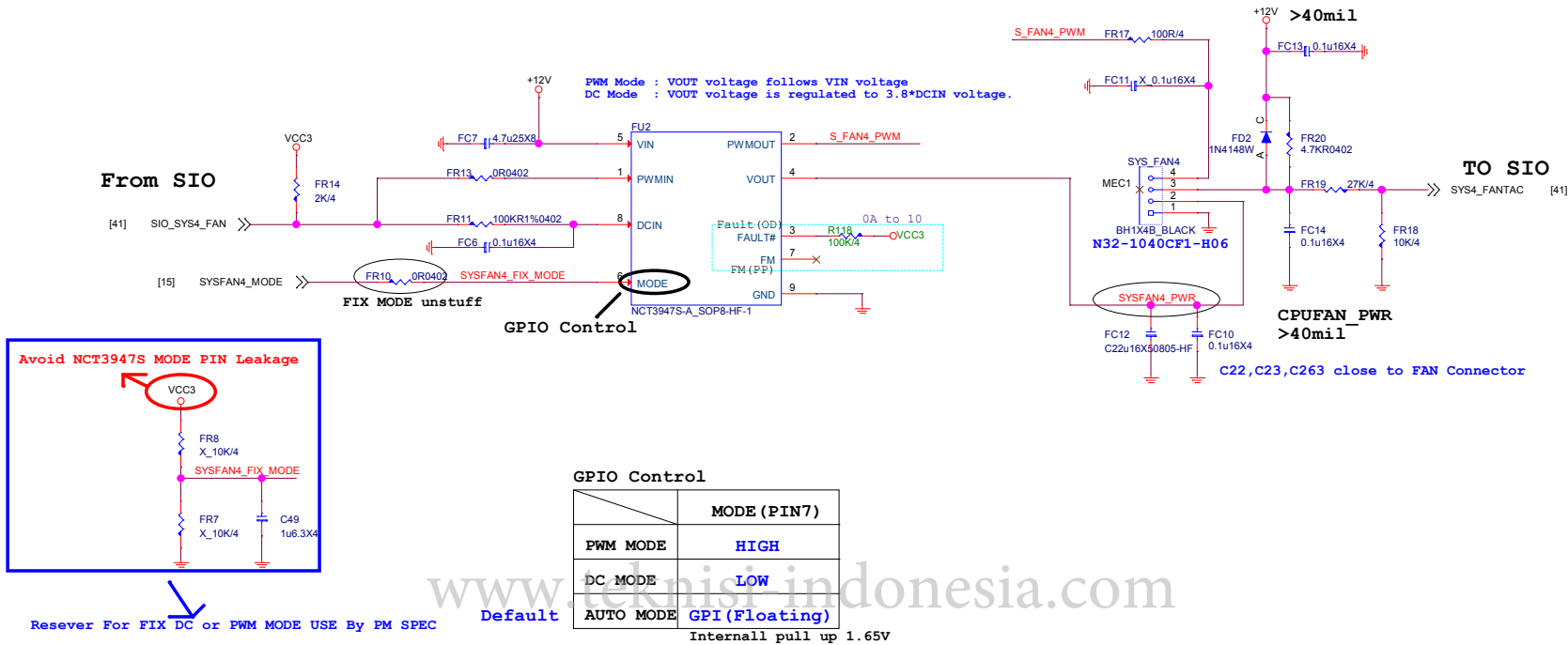


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

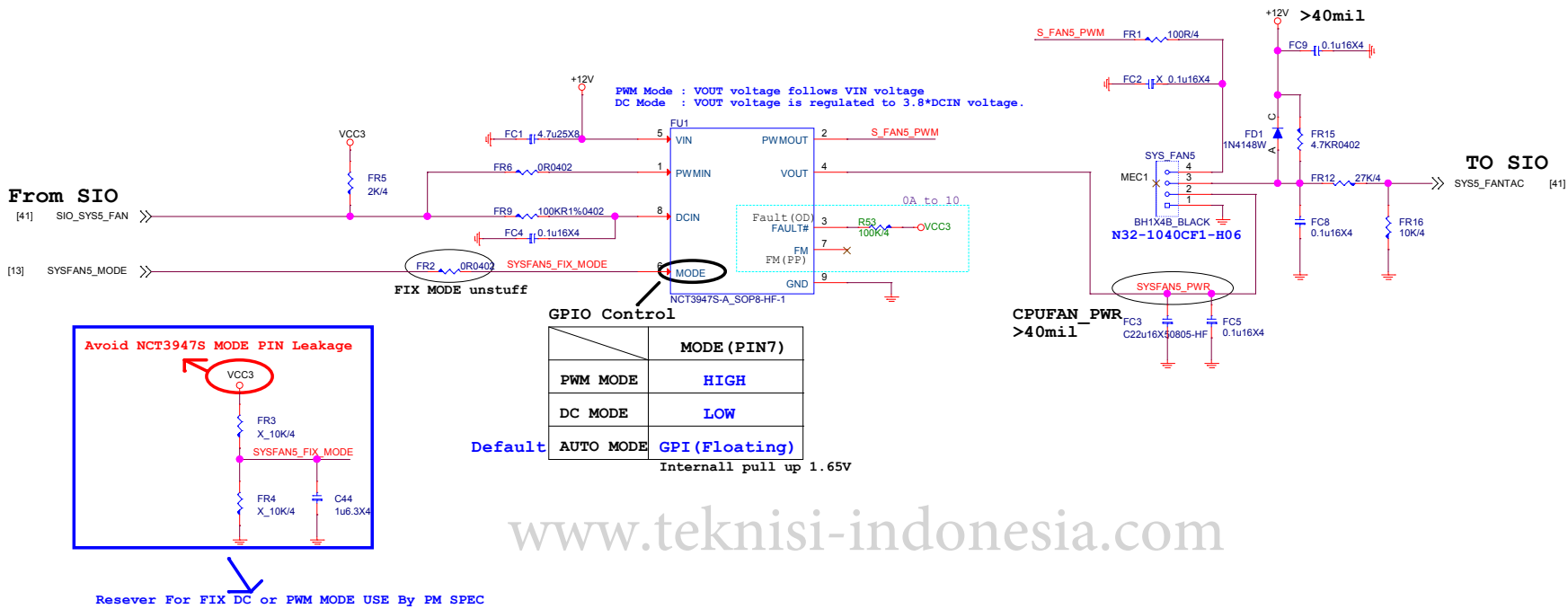


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

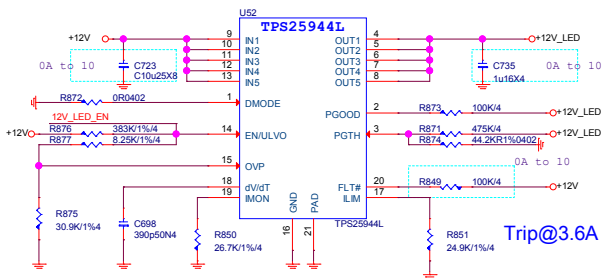


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Delete ALL Audio LED BY Spec Change 2018/4/19

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## JLED



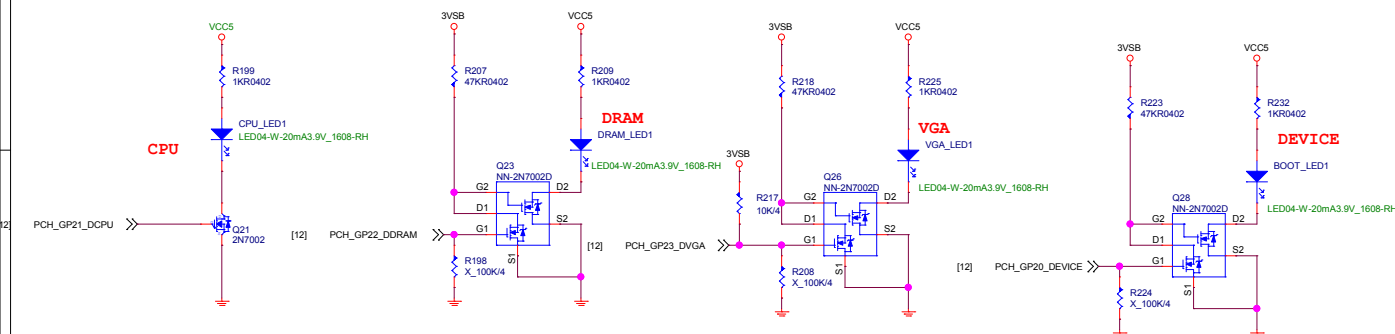
2017/7/28  
Based on "MSI-Header\_20170712",  
pin header(1x4) change to JRGB1 from JLED1

Delete ALL Audio LED BY Spec Change 2018/4/19

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## EZ DEBUG

白 : M:D0C-040T200-H91/ S:D0C-040S200-E07\*4



GPIO LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

msi MICRO-STAR INT'L CO., LTD.

Title RGB/AUDIO/EZ DEBUG LED

Size Document Number MS-7B98..

Date Thursday, May 17, 2018 Sheet 51 of 73

Nov 10

關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. 因此最後正常順利開機後，三個LED燈都是減掉的。

(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

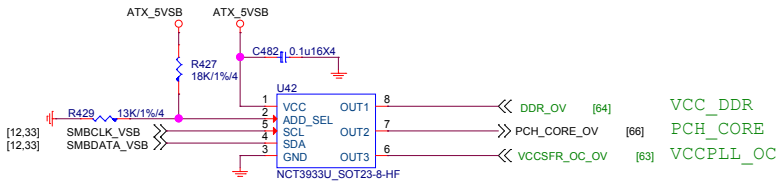


A schematic diagram showing a capacitor labeled C581 with a value of X\_10u6.3X6. The capacitor is connected between a terminal labeled VBAT and a ground symbol.

[illegible]

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



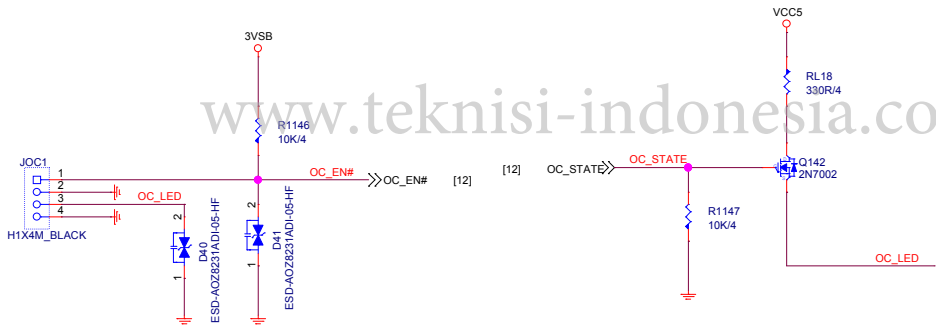
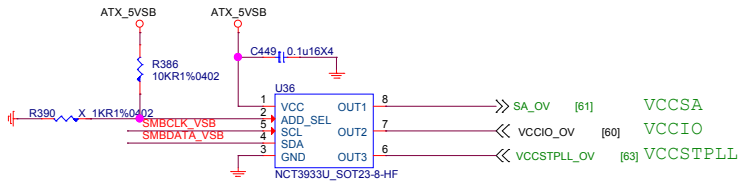
UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

UPI VOLTAGE CONSOLE

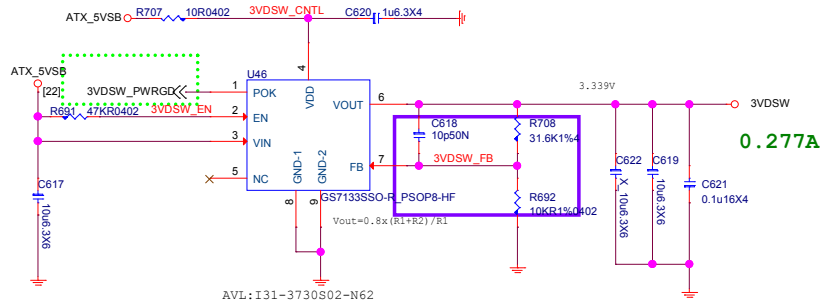
0x20:RH=10K,RL=OPEN



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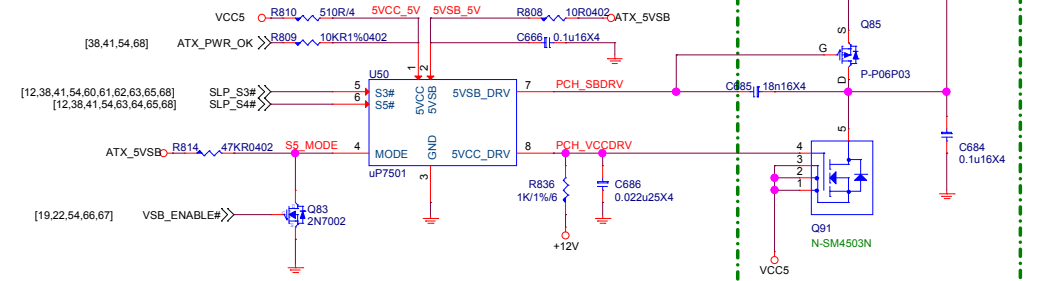
Title	OV-NCT3933/OV		
Size	Document Number	Rev	
	MS-7B98..	10	
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## 3VDSW

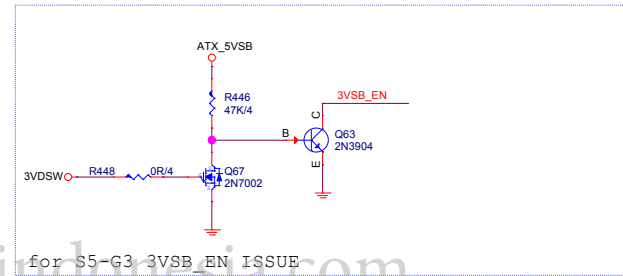
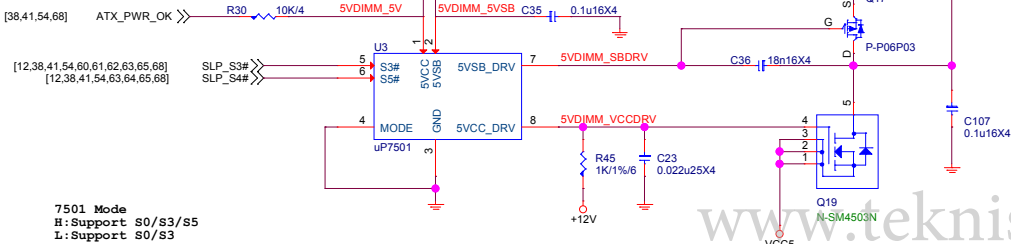


## 5VDUAL

5VDUAL is power source of 1P0SB

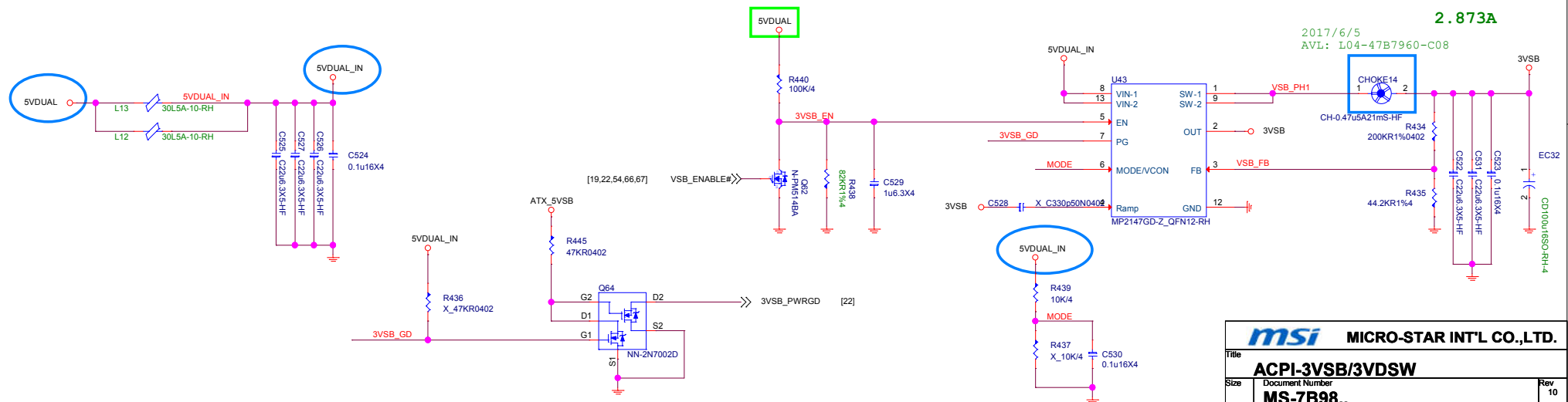


## 5VDIMM FOR DDR

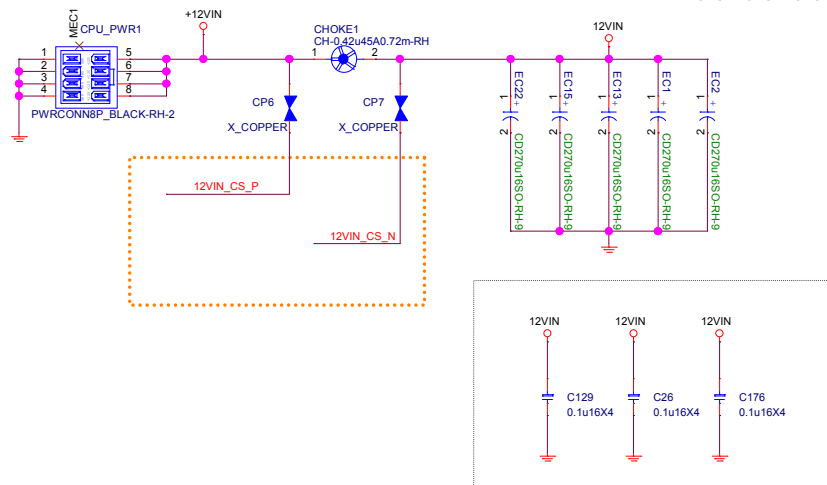
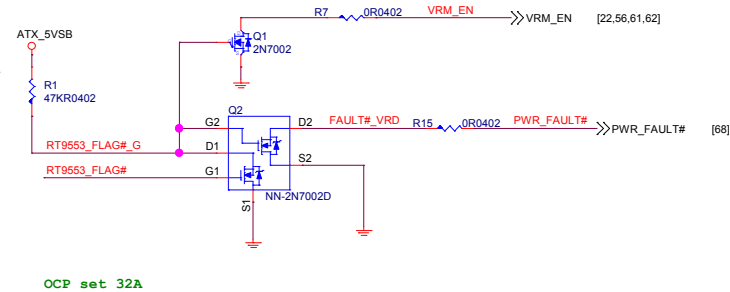
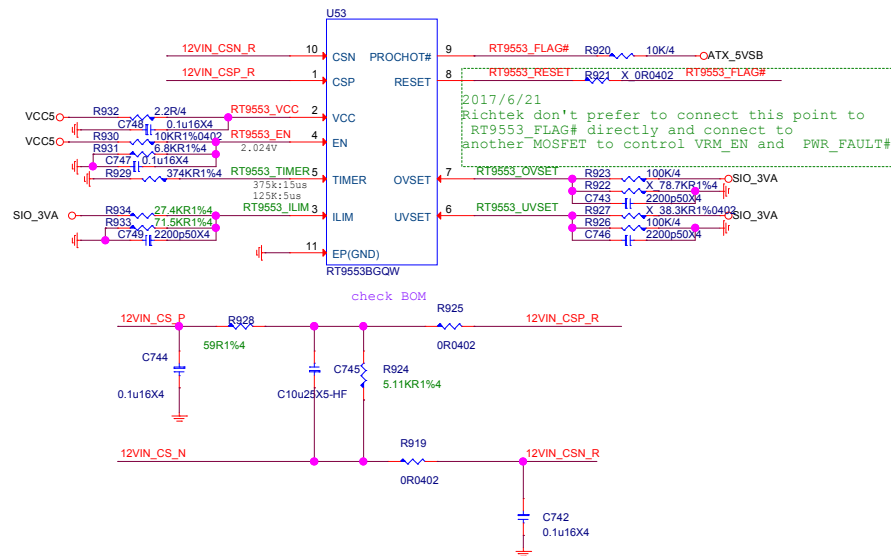


## 2.873A

2017/6/5  
AVL: L04-47B7960-C08



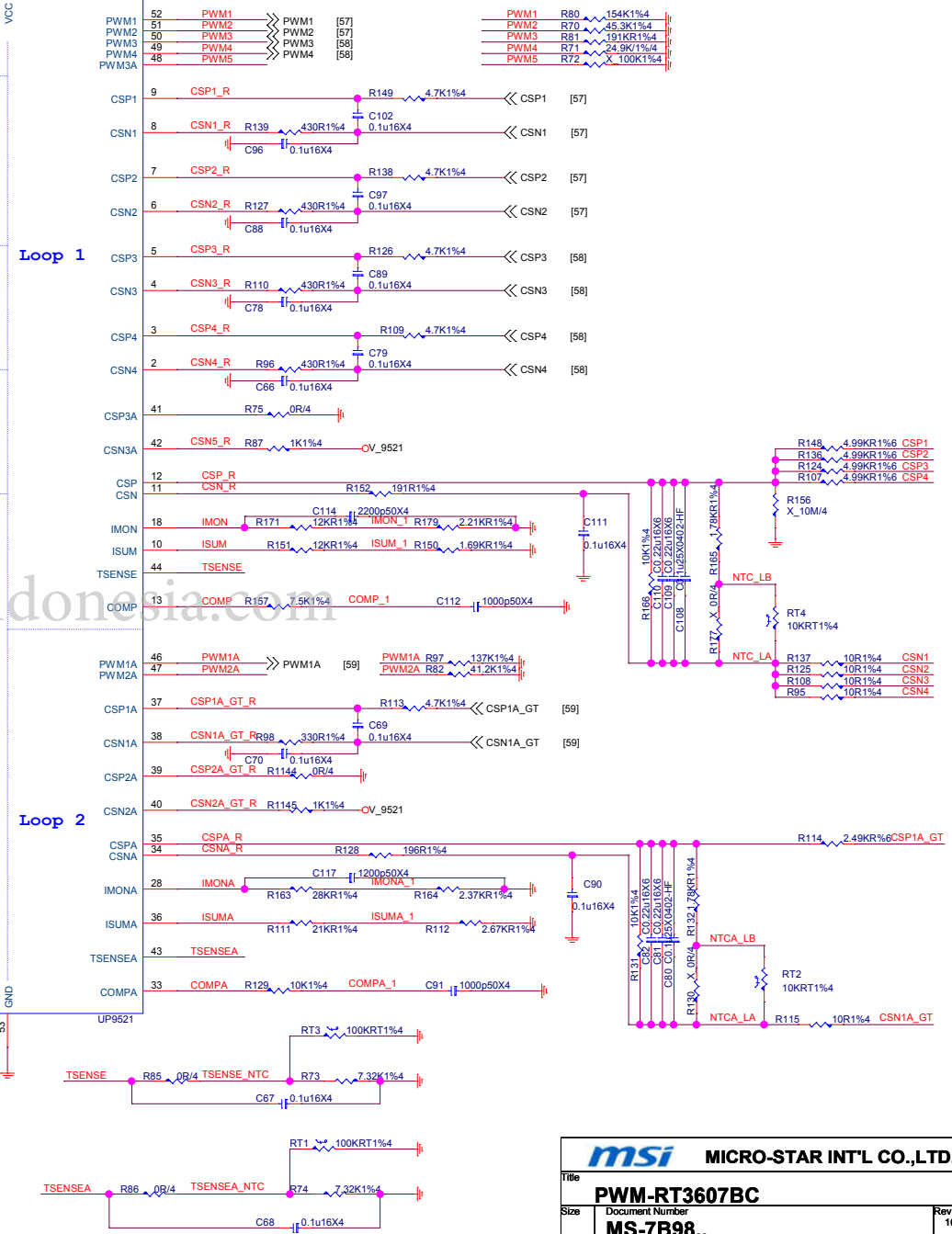
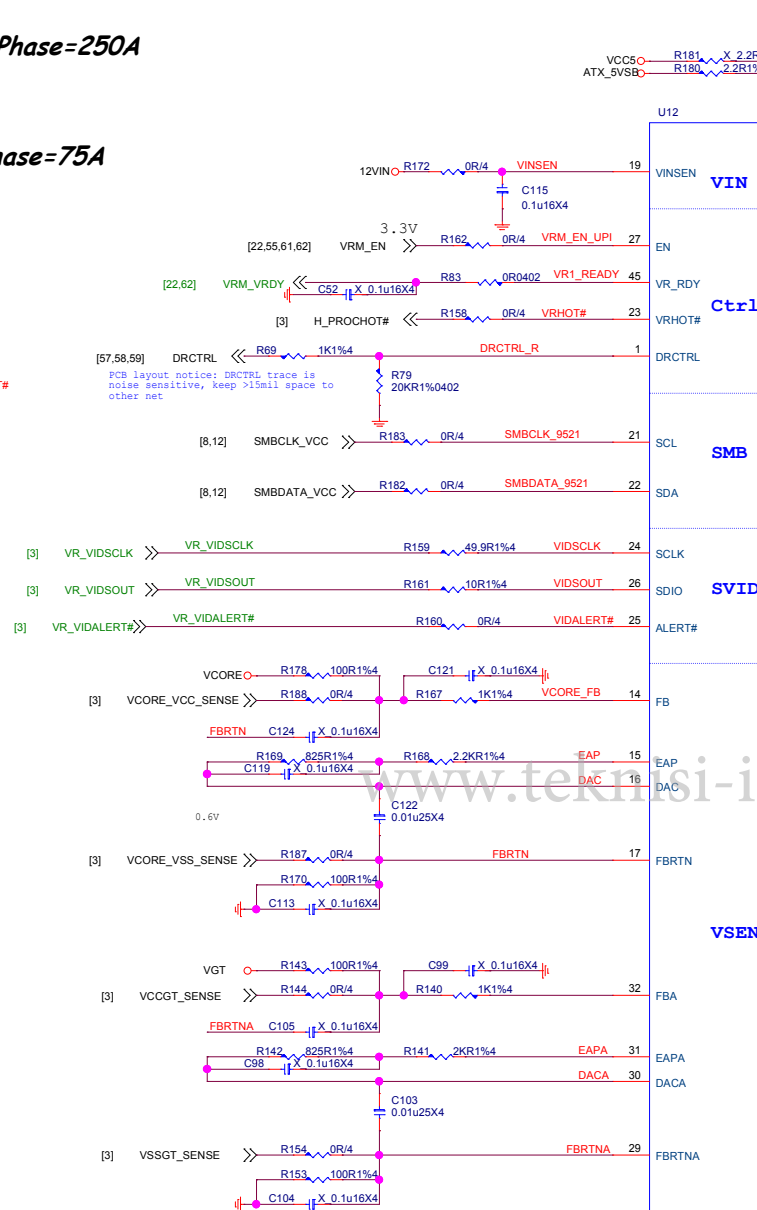
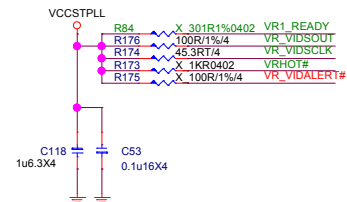




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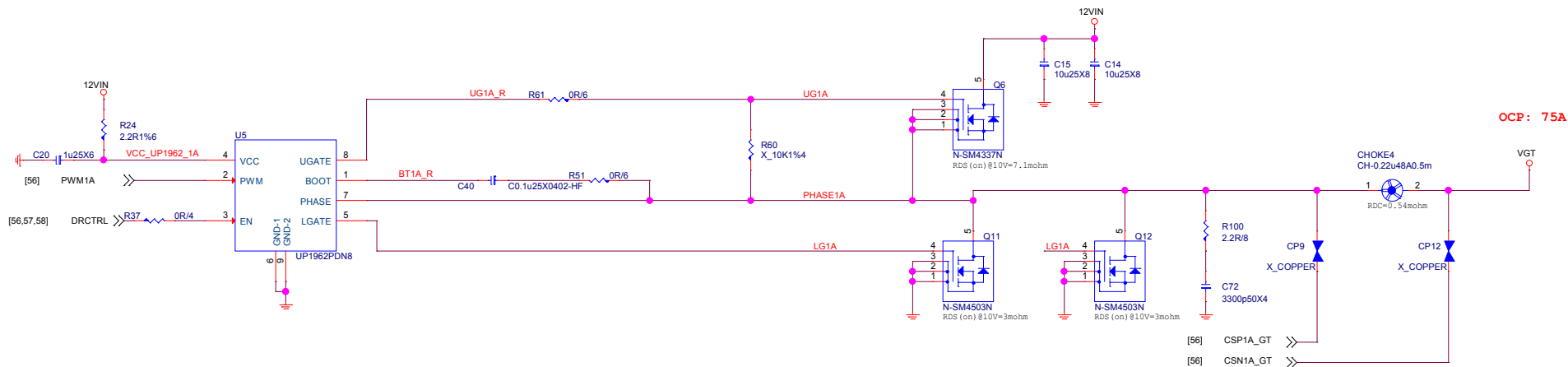
Vcore: ICC Max 193A  
LL: 1.6 mohm  
OCP: 62.5(Per-Phase)\*4Phase=250A

VGT: ICC Max 45A  
LL: 3.1 mohm  
OCP: 75A(Per-Phase)\*1Phase=75A



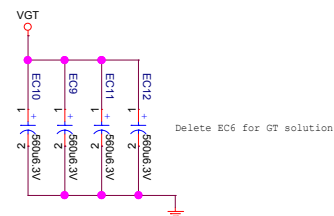




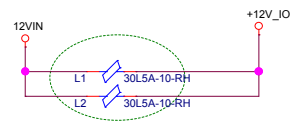


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Delete VGT 1 Phase 20180425



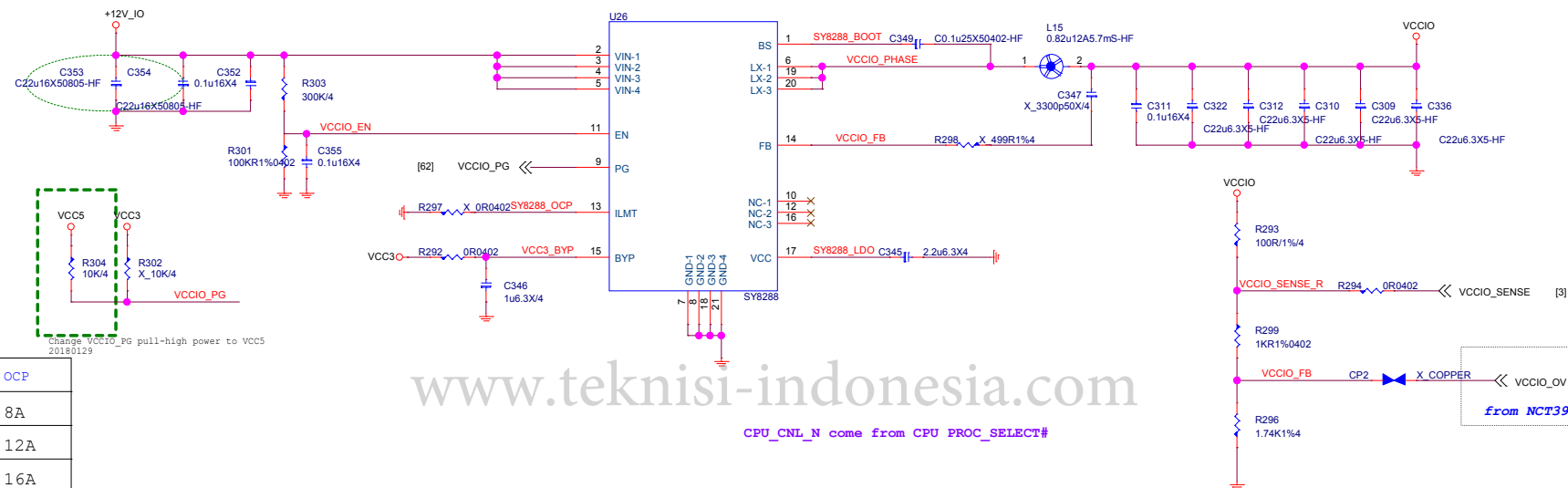
IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.



```

95W
ICCMAX=6.4A
Irms = 1.728A

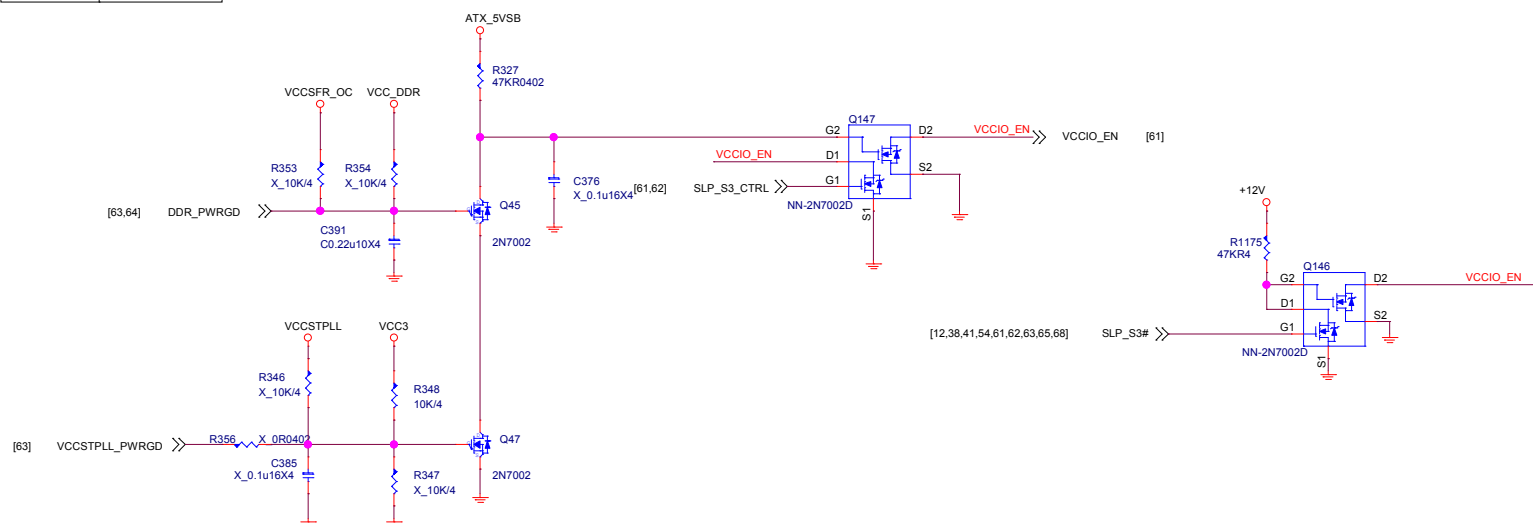
```



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

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CPU CNL N come from CPU PROC SELECT#



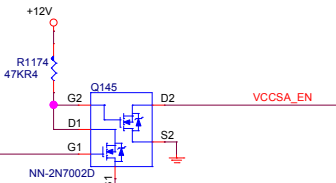
# SA Power:1.05V

1.05V; 11.1A

OCp = 11.1\*1.4=15.54A  
 Rocset = 1.4 \* Imax \* Rdson(low) / Iocset  
 = 1.4 \* 11.1 \* 3.3mohm / 10uA  
 = 5.12K (BOM上5.1K)

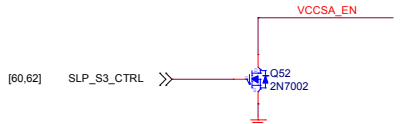
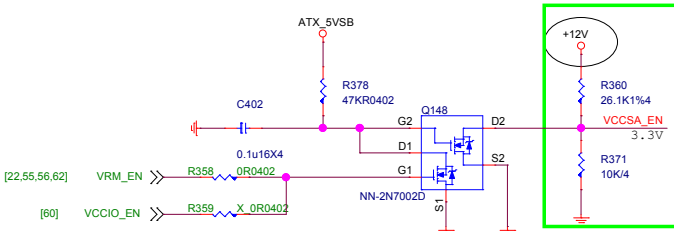
Rdson (low) 10V  
 D03-4503N0C-ST8 : 3mohm

2014.12.25  
 for up1540:C39 is OCP set min:5K ohm  
 stuff 5.36K OCP SET:15.76A



2014.08.21 update

Pull up by layout&Check level



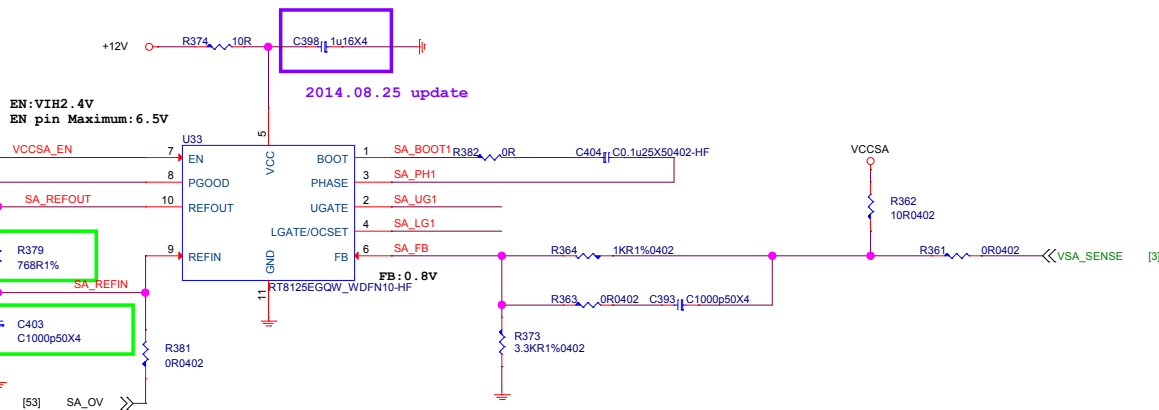
SLP\_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP\_S3# assertion to VR disabled  
 max:1us

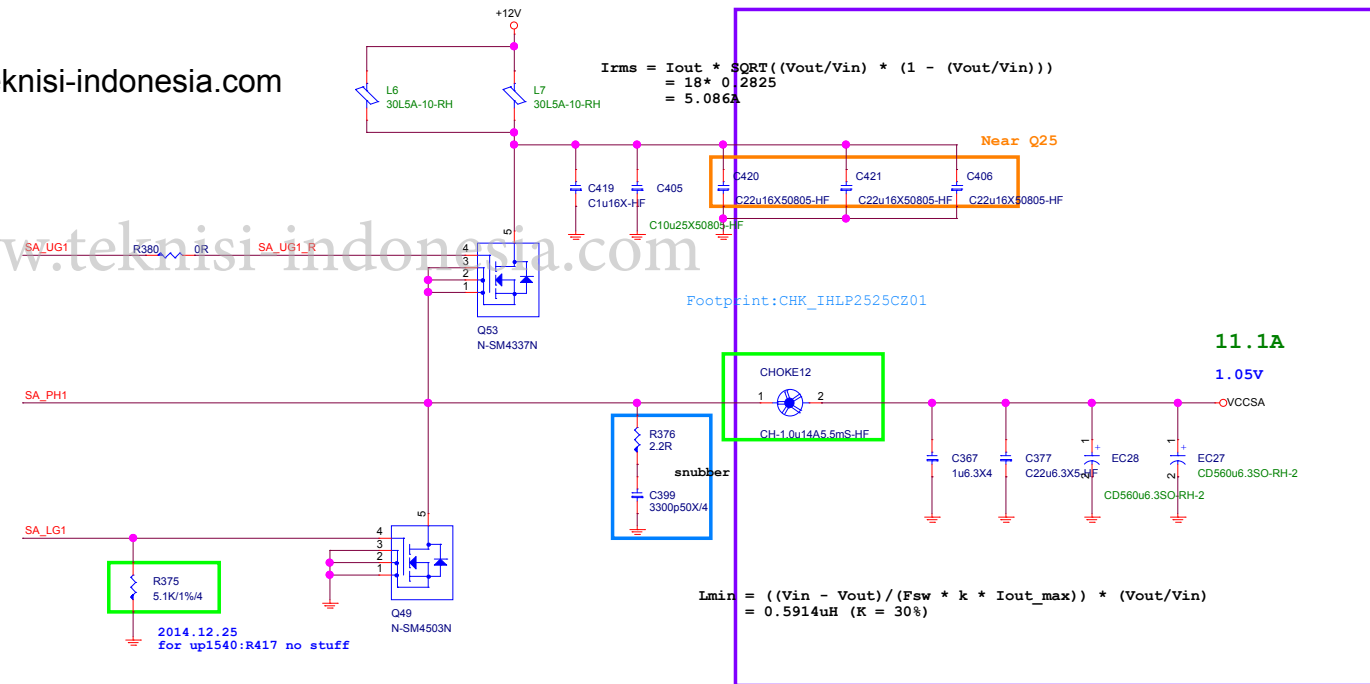
EN:VIH2.4V  
 EN pin Maximum:6.5V

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2014.08.25 update



$$I_{rms} = I_{out} * \sqrt{\frac{V_{out}}{V_{in}} * (1 - \frac{V_{out}}{V_{in}})}$$

$$= 18 * 0.2825$$

$$= 5.086A$$

Footprint:CHK\_IHLP2525CZ01

11.1A

1.05V

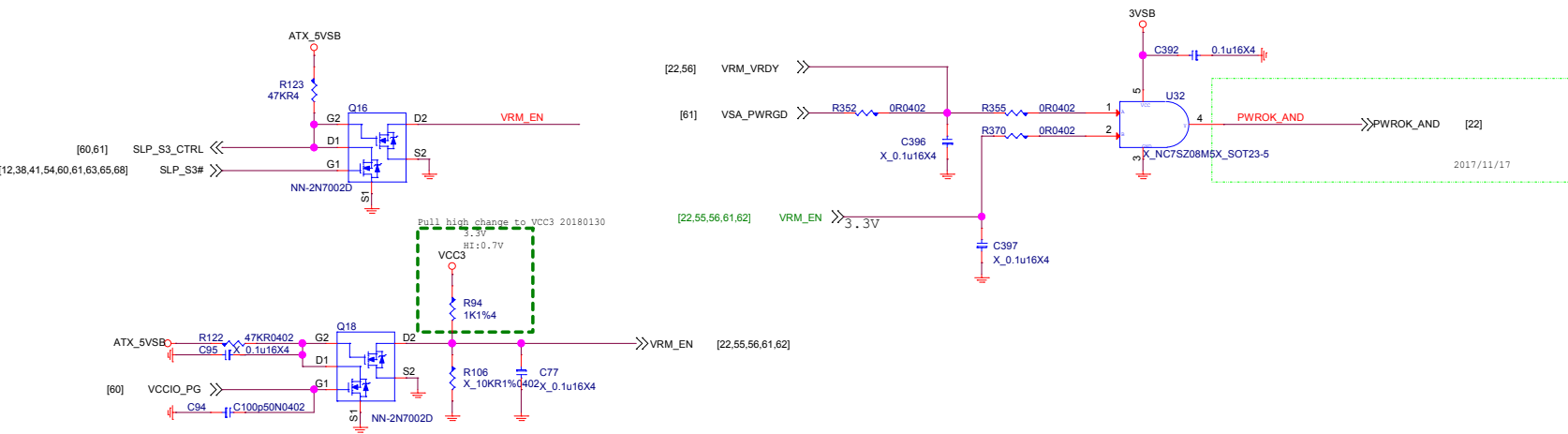
$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out} / V_{in})$$

$$= 0.5914uH (K = 30\%)$$

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Rev	10		

Sequence



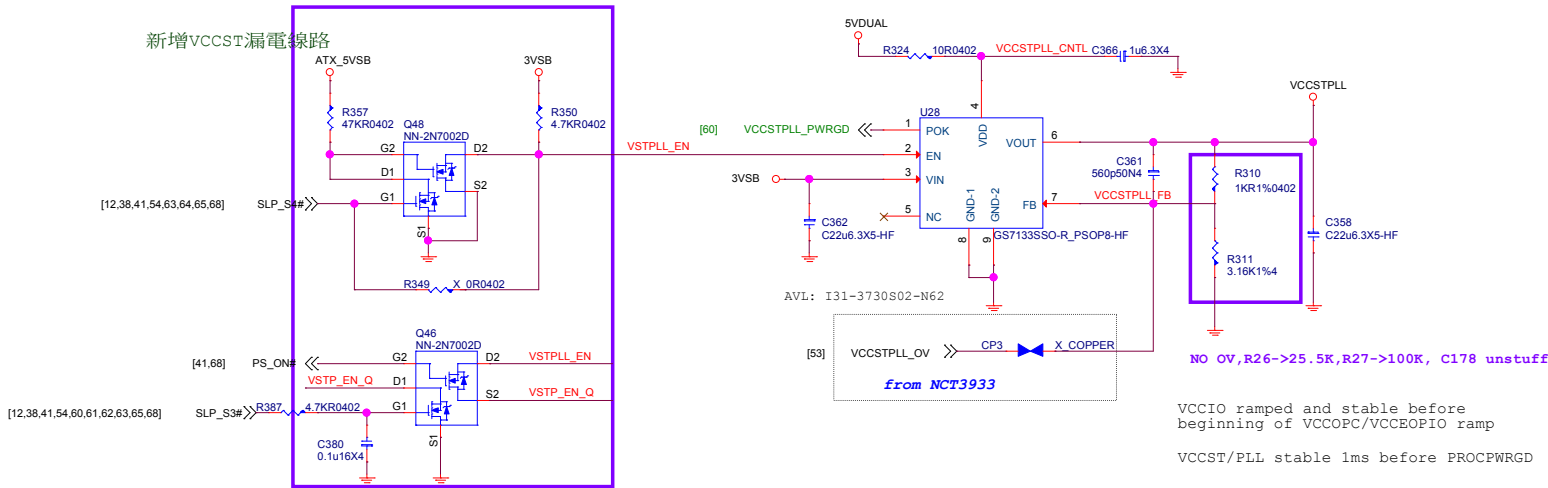
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## VCCSTPLL

1.05V; 230mA

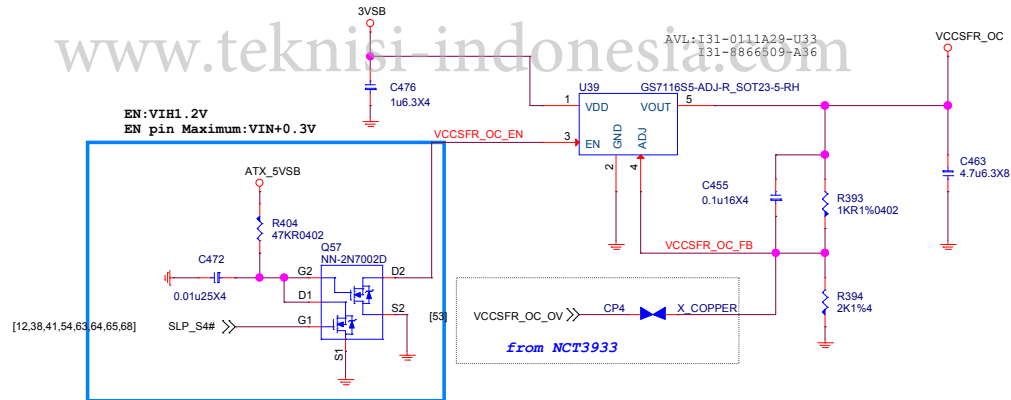
For Cost down VCCST&VCCPLL merge



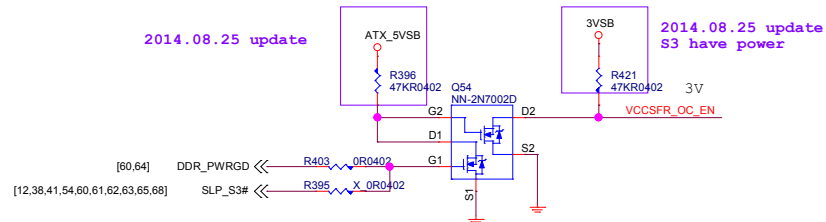
## VCCPLL OC

1.2V; 130mA

2014.08.21 update



2014.08.25 update



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CPU PWR-VCCST/PLL			10
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	MS-7B98..		
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**OCP 27.58**

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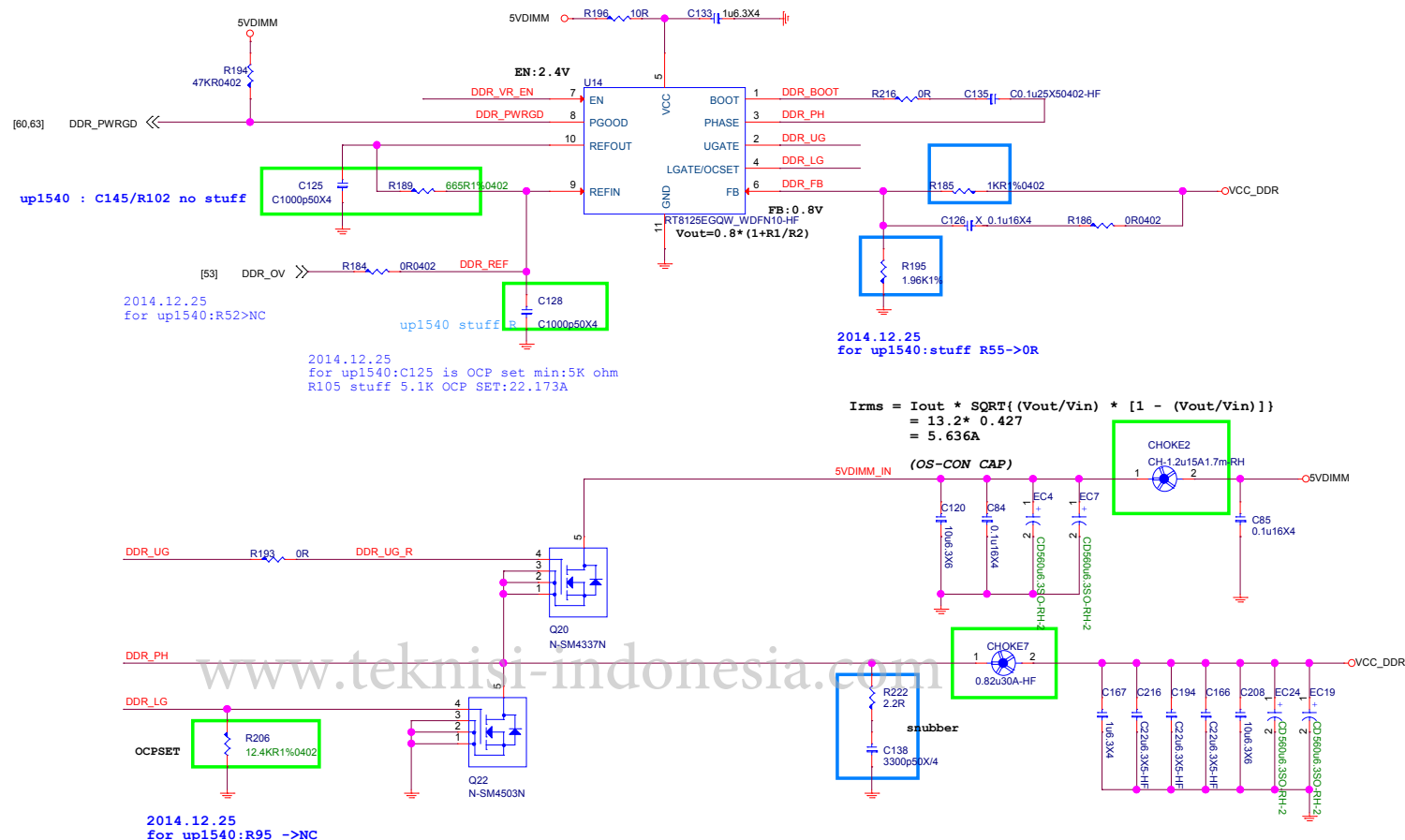
### 3.3A FOR CPU

**15.7A FOR 4DIMM**

0.5A FOR DDR  
VTT

$$\text{OCP} = 19.7 \times 1.4 = 27.58 \text{ A}$$

```
Rocset = 1.4 * Imax * Rdson(low) / Iocset
        = 1.4 * 19.5 * 4.6mohm / 10uA
        = 12.6K (BOM上12.4K)
```



2014.12.25  
for up1540:R95 ->NC

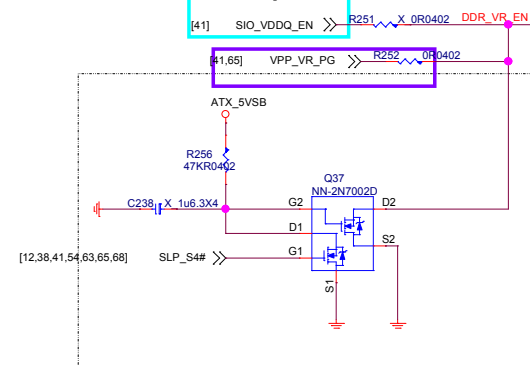
Datasheet公式計算

$$\begin{aligned} L_{\min} &= ((V_{\text{in}} - 1.2V) / (F_{\text{sw}} * k * I_{\text{out\_max}})) * (V_{\text{out}} / V_{\text{in}}) \\ &= 0.7677\mu\text{H} \quad (K = 30\%) \end{aligned}$$

若帶入CAP ESR計算,  $0.2432\mu\text{H} < L < 1.2897\mu\text{H}$

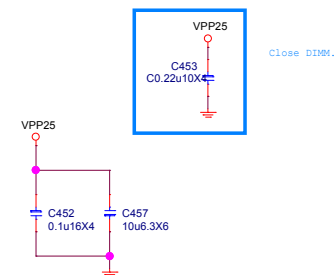
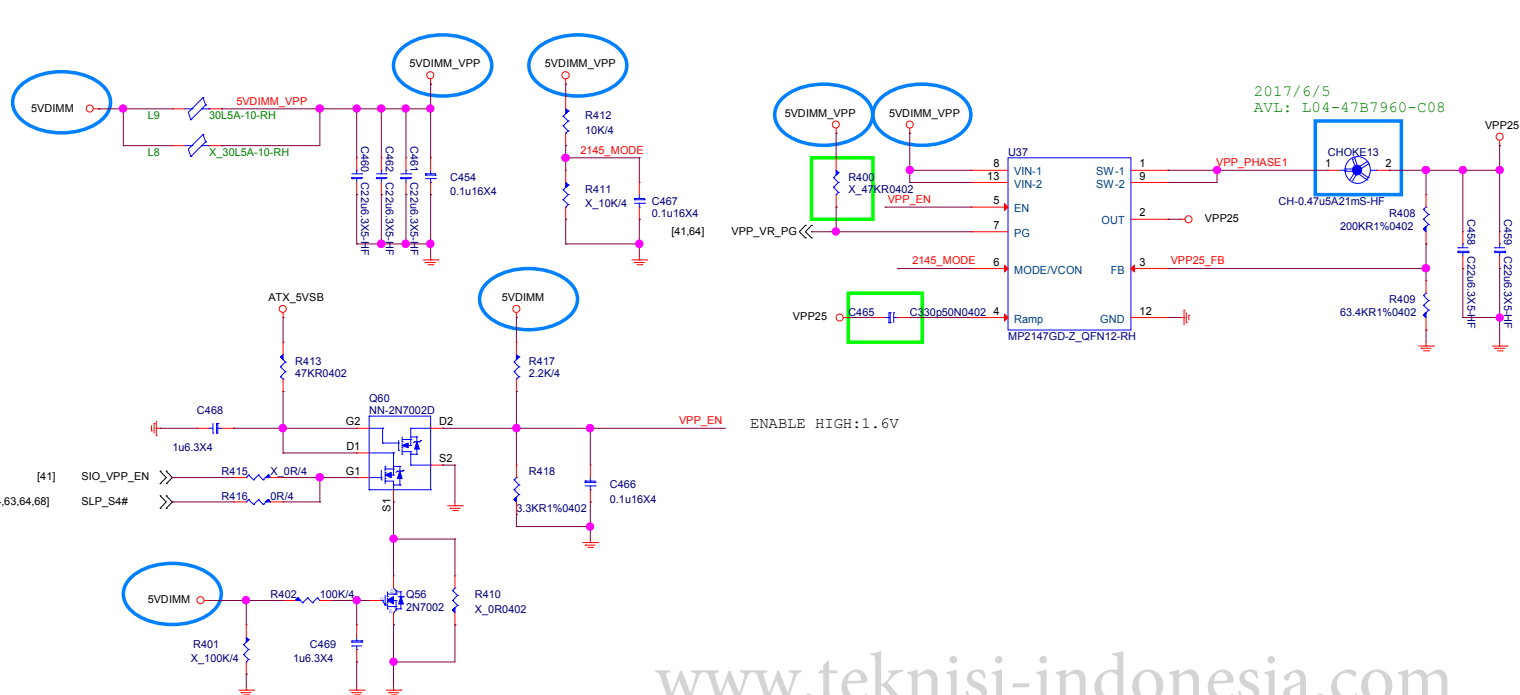
2014.12.17 update

From SIO pin 87



# 4DIMM :2.24A FOR DDR VPP2.5V

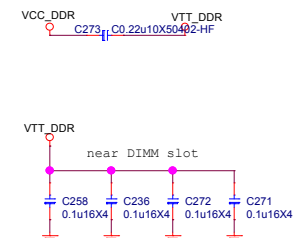
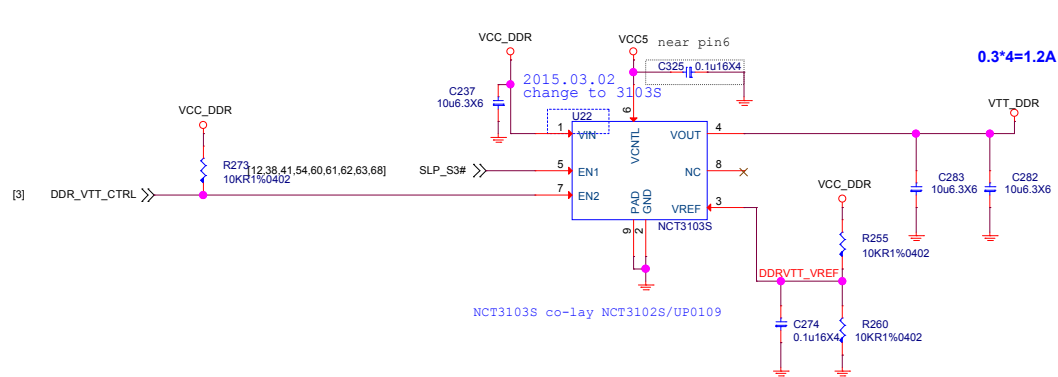
## VPP25 Power 2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

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## DDR VTT Power



## PCH 1VSB

1.05V; 13.36A

Rdson(10V) 4.5V

D03-3116M00-U47 : 3.6 mohm

D03-632BA0C-N03 : 4.6mohm

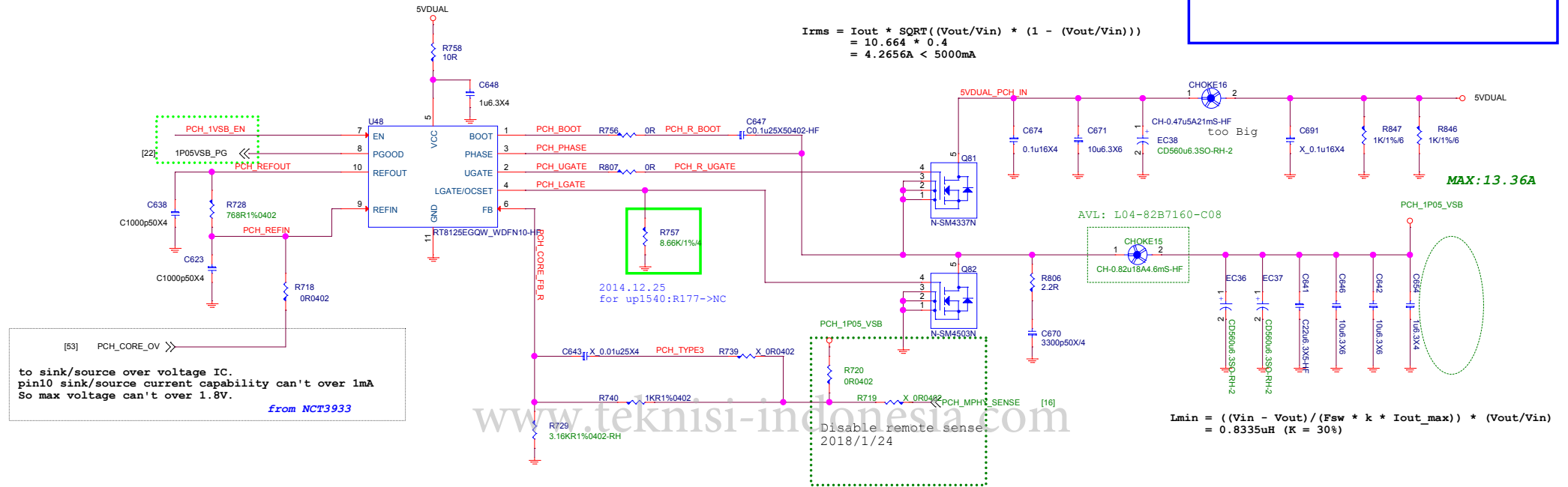
D03-3056M00-U47 : 6.2mohm

OCP = 13.36\*1.4=18.704A

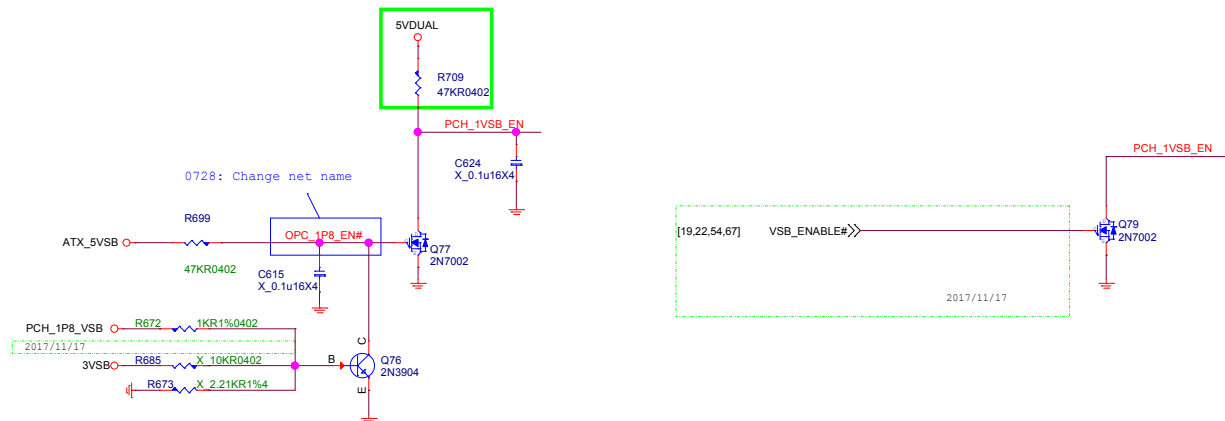
Rocset = 1.4 \* I<sub>max</sub> \* Rdson(10V) / Iocset  
= 1.4 \* 13.36 \* 4.6mohm / 10uA  
= 8.6K (BOM 8.66K)

Change to Choke (L04-47B7930-M26) form bead

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))} \\ &= 10.664 * 0.4 \\ &= 4.2656A < 5000mA \end{aligned}$$



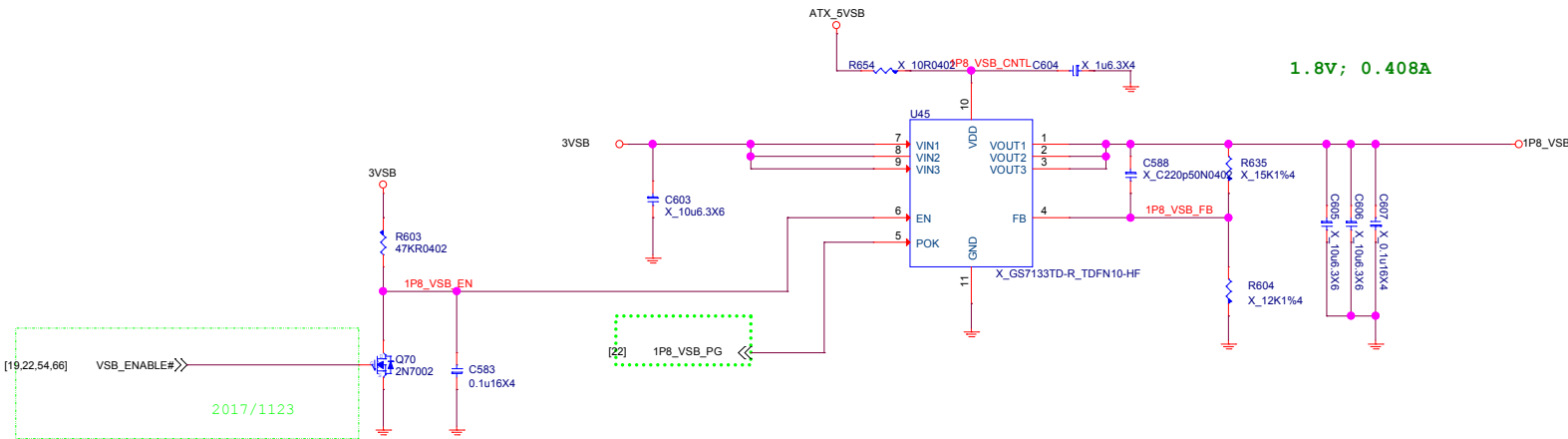
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$$\begin{aligned} L_{min} &= ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out}/V_{in}) \\ &= 0.8335uH (K = 30\%) \end{aligned}$$

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Delete due to USB retimer use external DC to DC schematic  
2018/01/17

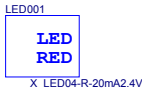
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ASM\_1P8\_VSB Delete ,due to drop ASM 1562

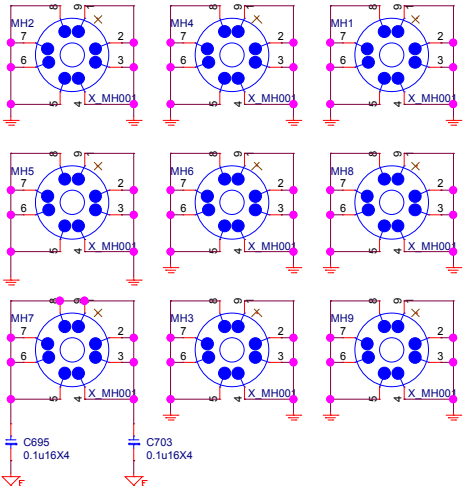




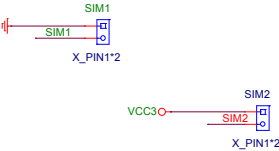
PK0-07B980A-G37, 精成-深圳, 23, 寶安恩斯邁廠 (MSIS)  
PK0-07B980A-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)



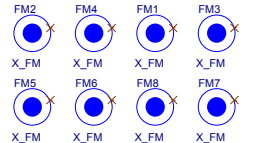
Mounting Holes



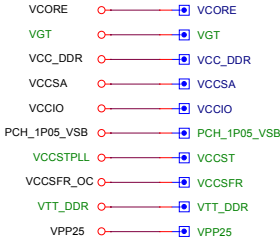
Simulation



Optical Fiducial Marks-120



Vcheck



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